Challenges ahead in designing embedded analog circuits in nanometer technologies

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- performance limitations in analog design
- design example
- evolution with scaling technology
- scalable analog blocks
- mixed-signal crosstalk analysis
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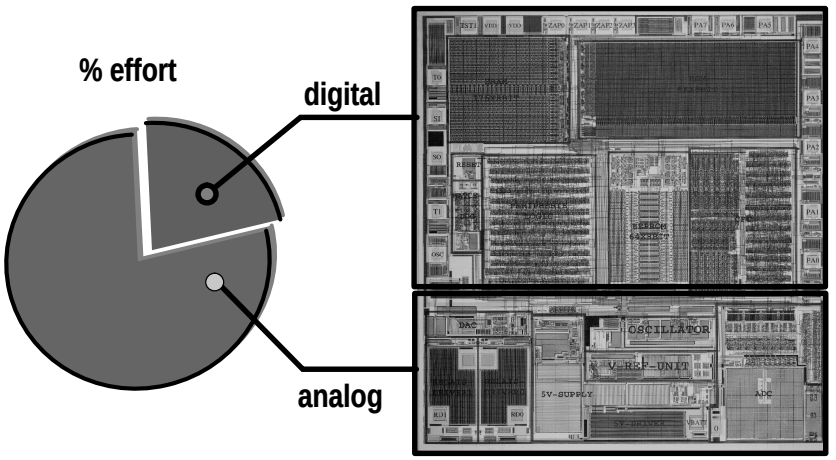
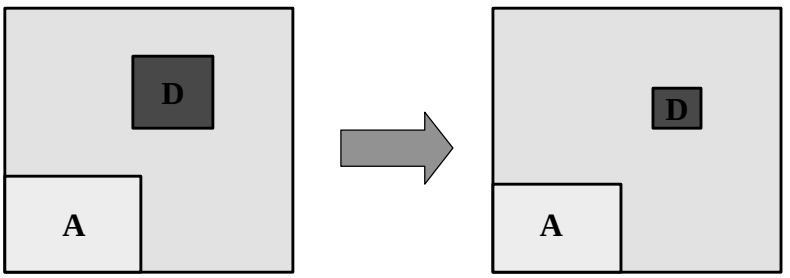
SoC example

commercial mixed-signal ASIC



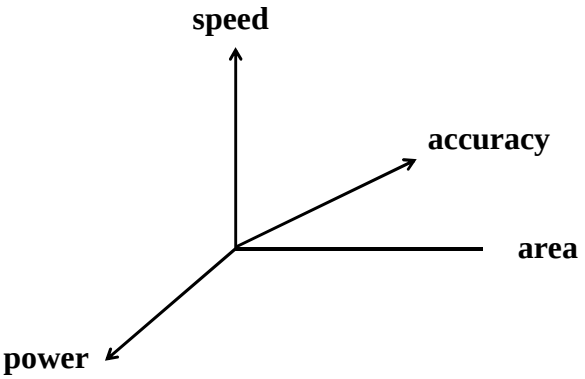
analog is bottleneck in mixed-signal design

Process scaling ?



- analog does not become smaller
- analog has problem with lower supply voltages
- embedding creates signal integrity problems

Performance limits to analog circuits



Limit 1 : Noise

$$P = 8kT\ f\ DR^2$$

[Vittoz AICSP 1994]

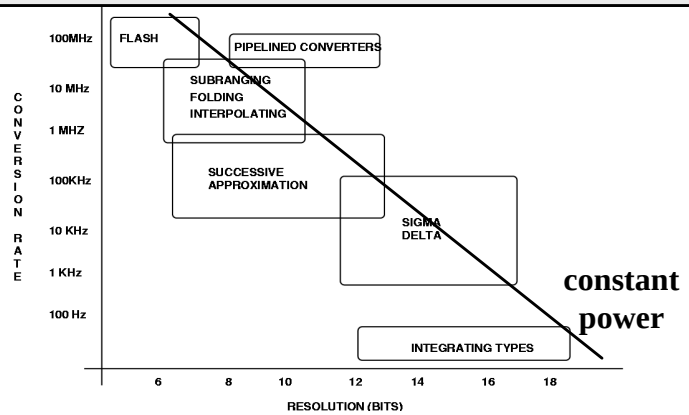
Limit 2 : Mismatch

$$P = 24\ C_{ox}\ A_{VT0}^2\ f\ DR^2$$

[Kinget CICC 1996]

Important basic trade-off

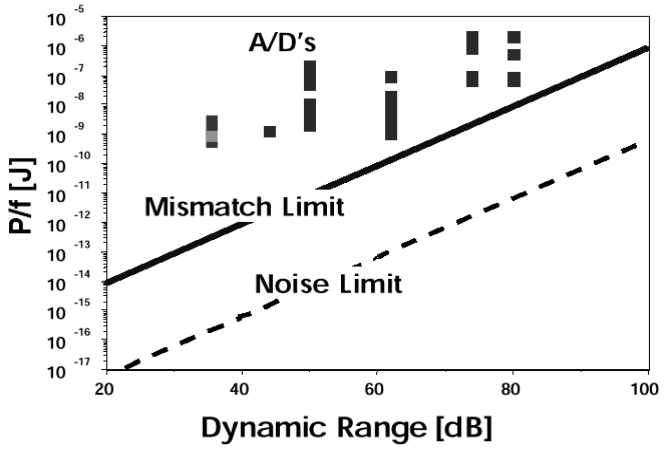
$$\frac{Speed * Accuracy^2}{Power} = techn\ const$$



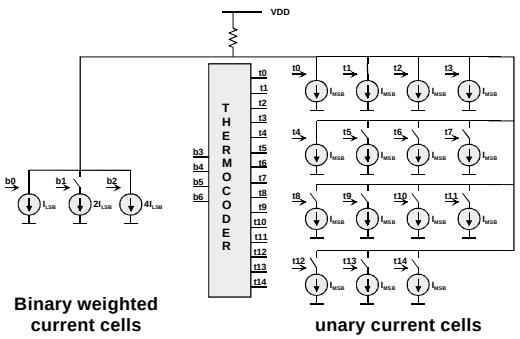
constant power

Systems : noise versus mismatch

- compare noise limit, mismatch limit and practical designs

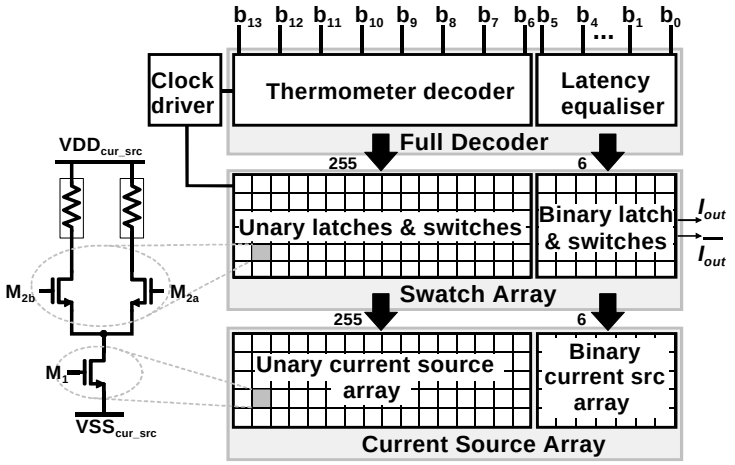


Design example : current-steering DAC

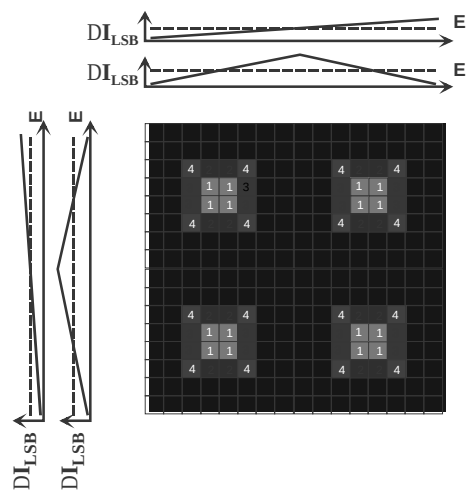


	Specification	Value	Value
Static	INL	LSB	
	DNL	LSB	
	Parametric Yield	%	
	Number of bits	-	
Dynamic	Glitch energy	pV.s	
	Settling time	ns	
	Sample frequency	MHz	
Environmental	Output range	V	
	R_{Load}	Ω	
	Digital levels	-	
	Power Supply	V	

CMOS current-steering DAC

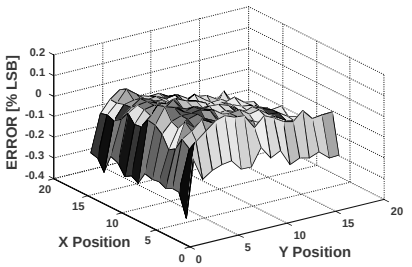


Static specifications: systematic errors



extracted profile

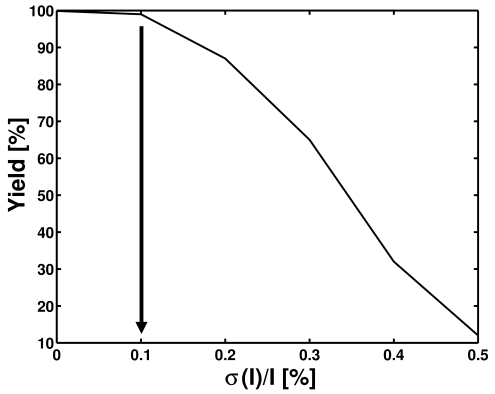
[Van der Plas ProRISC 2000]



compensation by Q^2 random-walk switching scheme

Static specifications : random errors

minimum transistor area is determined by the yield (INL < 0.5 LSB) through mismatches :



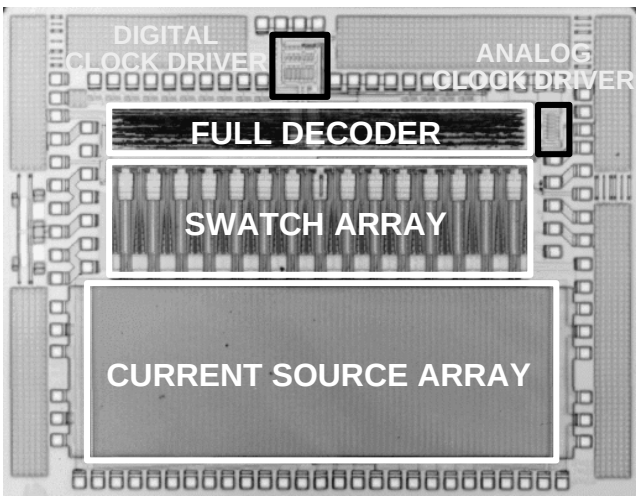
for yield > 99.7 %

$$\frac{s(I)}{I} < 0.1\%$$

Layout of the 14-bit D/A converter

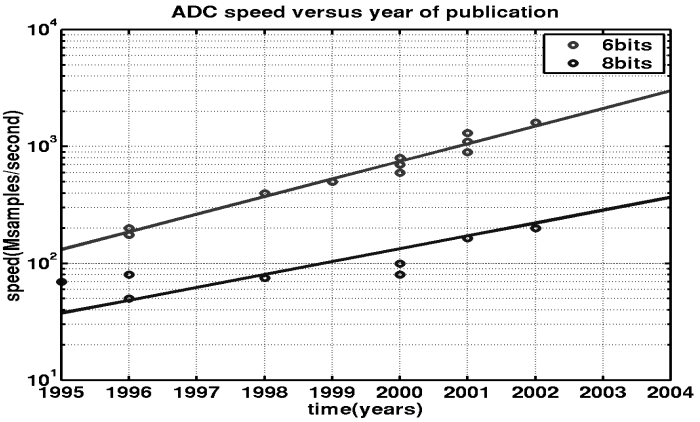
[Vandenbussche ISSCC'99]

intrinsic 14-bit INL
150 Msamples/s
0.5 µm CMOS



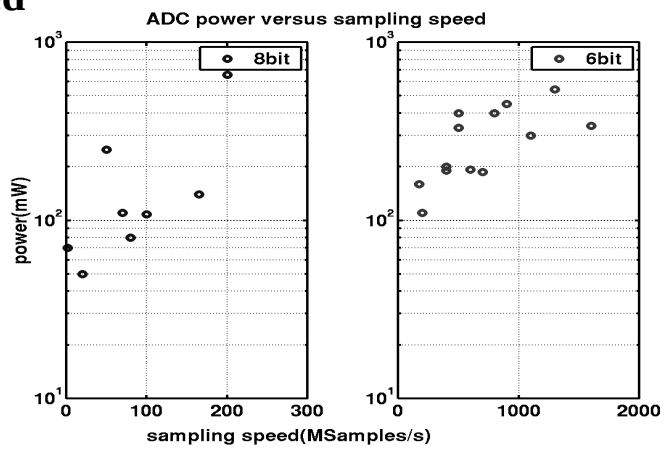
ADC evolution : speed

- **increase of sampling frequency follows almost Moore's law**



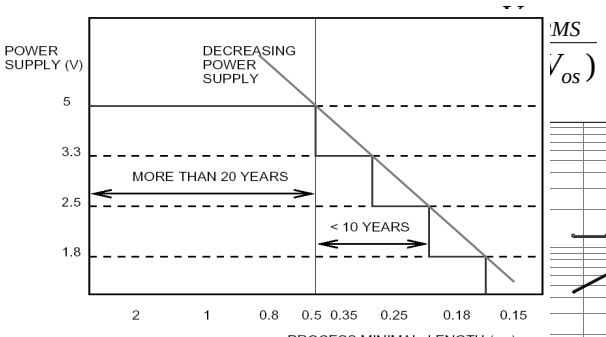
ADC evolution : power

- **power of ADC mostly directly proportional to speed**



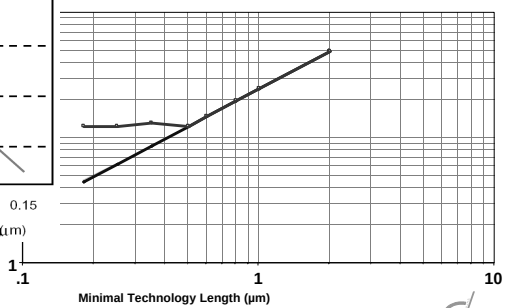
Impact of mismatch and Vdd scaling

- maximum input range reduces
- for fixed resolution : offset requirement more important



$\left(\frac{MS}{V_{os}}\right)$

$$P = 24\, C_{ox}\, A_{VT0}^2\, f\, DR^2$$

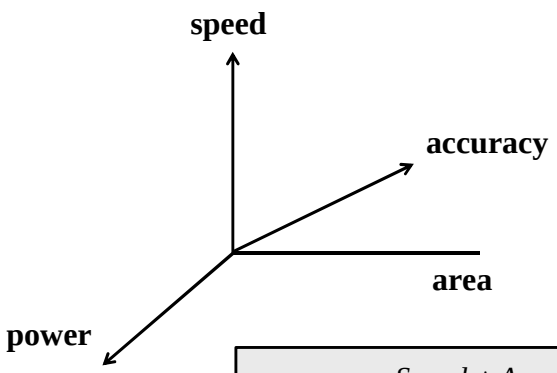


[fixed resolution]

Scalable analog blocks

- **motivation :**
  - multi-mode operation
    - e.g. mix telecom standards, 4G, MIMO
  - dynamic operation :
    - adapt to situation
      - e.g. battery levels
    - adapt to signals
      - e.g. blockers, crest factor
  - preserve close-to-minimum power with minimum area overhead

Scalable analog blocks

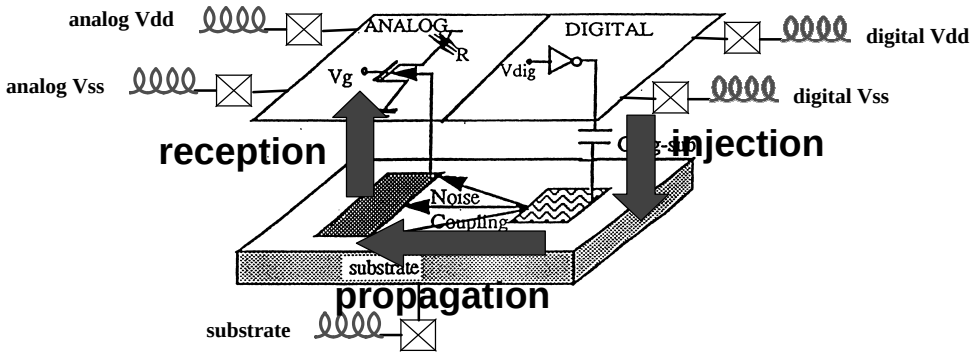


- ~~adapt Vdd~~
- adapt speed
- adapt accuracy
- through reconfiguration

$$\frac{Speed * Accuracy^{2}}{Power} = techn\ const$$

Supply/substrate noise coupling problem

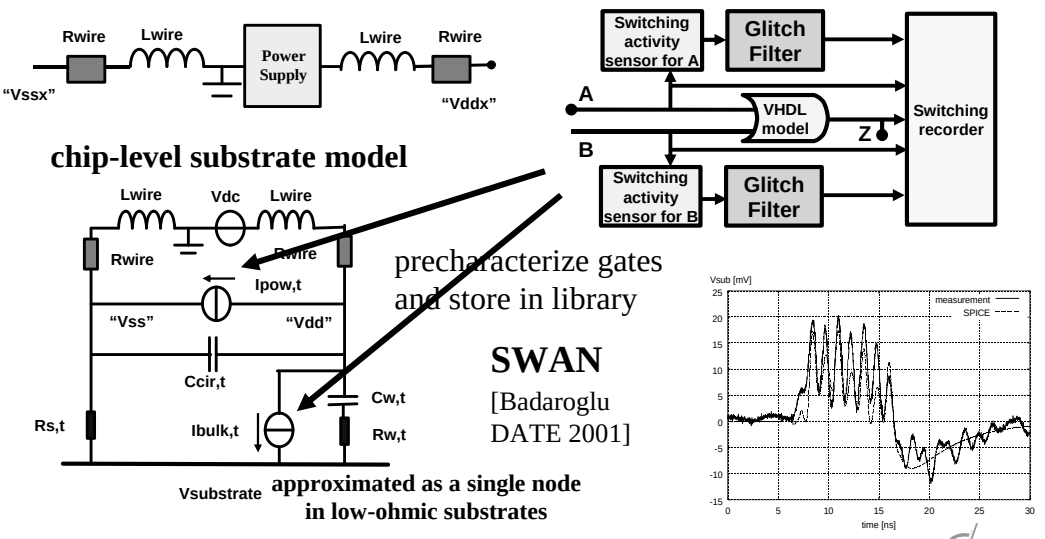
- noise is coupled through the supply lines and through the common substrate



Sources of substrate noise generation

- **inductive noise (di/dt, 100 mV)**
  - bonding wires
  - large di/dt on power supplies
  - non-ideal power supplies connecting directly to the substrate
- **capacitive coupling (dv/dt, 10 mV)**
  - interconnect capacitance to substrate
  - junction capacitances
- **impact ionization (Idrain, Vgs & Vds, 2 mV)**
  - high electric field near the drain of saturated MOS devices
  - substrate current injection

Substrate noise coupling analysis



[in cooperation with IMEC]

Switching noise impact on ADC

- **calculate noise impact on the SNR or ENOB of an embedded ADC**
  => equivalent to extra jitter due to subnoise
- **calculations 8-bit ADC based on measurements :**
  - SNR_Q : 49.93 dB
  - SNR_Q+J : 27.59 dB

$$Err_{jrms} = (\sqrt{8 \cdot p} \cdot f_{in} \cdot s_T) \cdot S_{rms}$$

$$Err_{qrms} = \frac{S_{rms}}{2^n \cdot \sqrt{6}/2}$$

$$N_{eff} = n - \log_2\left(\sqrt{1 + \left(\frac{Err_{jrms}}{Err_{qrms}}\right)^2}\right)$$

$$SNR = 20 \cdot \log\left(\frac{S_{rms}}{\sqrt{Err_{jrms}^{\ 2} + Err_{qrms}^{\ 2}}}\right)$$

[T. Wakimoto et al. JSSC 1988]

Conclusions

- **SoC's require solution for**
  - managing large complexity
  - increasing analog circuit productivity
  - avoid mixed-signal crosstalk
- **performance limits for analog circuits**
  - mismatch, noise, jitter
  - area does not scale, power may even go up
- **need for scalable/reconfigurable analog blocks**
- **mixed-signal verification and signal integrity**
  - parasitic crosstalk, supply/substrate noise, EM couplings...