System-level Stimuli Generation for the CELL Processor

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Agenda

- The CELL architecture (again)

- System-level verification challenges

- A system-level stimuli generation solution: X-Gen

- Results
The CELL Processor

The CELL Processor consists of multiple processing units, including SPU (Synergistic Processing Unit), LS (Load Store Unit), MFC (Media Fusion Controller), PPE (Power Processing Element), L2, and EIB (Execution Interconnect Bus). The diagram illustrates the interconnected components and the flow of data between them. The diagram also highlights the x8 configuration, indicating the parallel processing capability of the CELL Processor. The IOIF BFM (Input/Output Interface BFM) is connected to the BIC/IOC (Block Interconnect Controller/IO Controller) and the Memory, facilitating communication with other cells or external I/O devices.
System verification background: where we come from

Mainline system development in IBM

- Power based eServers: pSeries (UNIX), OpenPower (Linux), iSeries (previously known as AS/400)
  - Based on Power3, Power4, Power4+, Power5, …
- PowerPC 970 based systems (blades, Apple)
- Mainframes: zSeries (previously S/390)

System verification

- Processor centric
- A highly complex memory sub-system: coherency and consistency issues
- Systems are not tied to a single software application
Challenge #1: heterogeneous processors

- A single PPE
  - Dual thread, 64-bit, PowerPC processor
- Eight SPEs
  - Synergetic Processing Element
  - 128-bit wide vector processor
- Other high-end systems in IBM are homogeneous
  - Typically multi-processor PowerPC systems
- Some MP-oriented verification tools cannot be used
Challenge #2: non-processor translation mechanism

- The PowerPC address translation mechanism is highly complex
- Supported by:
  - The PPE - A PowerPC
  - The MFC - essentially a DMA
- These mechanisms are usually well-verified before the system-level
  - Using state-of-the-art processor verification tools
- But: the MFC is not a processor
  - Some of the load was passed to the system level
- Required SL tools to go into finer details
Challenges 3, 4, and 5

- A completely new architecture
  - Combines of relative instability and high complexity

- Coherency and consistency are still crucial: the PPE, SPEs are all coherent
- The CELL is general purpose
  - Doesn’t aim at a single software application
  - As opposed to more application specific SoCs
Simulation-based functional verification

- Stimuli Generator
- Stimuli (test-case)
- HDL Model
- HDL Simulator
- Checking
System-level stimuli generation solution

- X-Gen: the same tool is used for high-end servers, the CELL, and other designs
- Reuse from other systems:
  - Abstract system model: >40%
  - Test requests: ~30%
- Possible due to the model-based test-generation paradigm
- Dummy configurations were used for verification in addition to 1xPPE – 8xSPE
  - All with the same set of test requests
CELL System verification results

- Close to 150 bugs exposed
- I spoke about stimuli generation: there’s also checking, coverage, *verification execution*, …