Introducing Mixed Signal into FPGA based MPSoC

Yankin Tanurhan
Sr. Director Application and IP Solutions
Actel Corporation
The Race to the Programmable System Chip

Analog Suppliers

FPGA Suppliers

Programmable System Chip

MCU Suppliers

ASIC Suppliers

```
cin >> X >> Y;
for (;;)
{cout <<"X,Y=?";
cin >> X >> Y; }
```
Fusion Project: World’s First Mixed Signal FPGA based MPSoC

Typical System

- System Memory: DRAM
- Cache Memory: SRAM
- NV Storage: FLASH
- MPU / MCU
- FPGA / ASIC
- Analog Interface
- Power Mgmt
- Clock Mgmt
- Discrete Analog

© 2005 Actel Confidential and Proprietary
Fusion Platform - Physical View

FPGA Fabric

System Application

Fusion Applet 1
Fusion Applet 2
Fusion Applet 3

Optional MCU
ARM or 8051

Peripheral in FPGA Fabric

Control

Fusion Backbone

Flash Memory (peripheral)
Analog Peripheral 1
Analog Peripheral 2
Analog Peripheral n

Optional MCU
ARM or 8051

Peripheral in FPGA Fabric
Level 0 – Fusion Peripherals

- Configurable, hard-wired, analog & flash blocks
- Optional peripherals in soft (FPGA) gates
- Standardized interface embedded in all peripherals

FLASH MEMORY

Analog Peripheral 1  Analog Peripheral 2  Analog Peripheral n  Peripherals in FPGA Fabric (i.e. logic, PLL, FIFO)
Level 1 – Fusion Backbone

- Fusion Backbone is Flexible Bus and Control Logic
- Built-in control (soft IP) configures peripherals based on information stored in flash memory
- Bus controls communication between peripherals

Fusion Backbone

- Analog Peripheral 1
- Analog Peripheral 2
- Analog Peripheral n
- Peripherals in FPGA Fabric (i.e. logic, PLL, FIFO)
Level 2 – Fusion Applet

- Application building blocks implementing specific functions
- Sourced by Actel, a customer, or a partner
- Soft IP implementation

![Diagram of Fusion Applet and Fusion Backbone with associated peripherals]

- Analog Peripheral 1
- Analog Peripheral 2
- Analog Peripheral n
- Peripherals in FPGA Fabric (i.e. logic, PLL, FIFO)
Level 3 – System Applications

- Larger user-application that combines applets
- Optional MCU enables a combination of software and HDL-based design methods

Optional ARM or 8051 processor

System Applications

Fusion Applet

Fusion Backbone

Analog Peripheral 1

Analog Peripheral 2

Analog Peripheral n

Peripherals in FPGA Fabric (i.e. logic, PLL, FIFO)
Fusion Architecture Stack

Benefits

- **Flexible design environment**
  - Layered model enables design at high or low levels of abstraction

- **Advantages**
  - Peripherals can be hard-wired resources or soft IP
  - Backbone is scalable to any number of Peripherals or Applets
  - Applets can be rapidly combined to create large applications
  - Well defined interface for external IP and tool integration
Integration increases complexity

- Tools needs increase with added integration
  - High-level design productivity
  - Hardware / software co-verification
  - Bus-based communication
  - Device / system modeling
  - Hardware and Software Debugging capability

- Innovative Fusion Tools resolve Complexity...
Development Flow

Design Start
- Actel IP Vault
- Configure IP Cores
- Stitch System Together

Actel IP

Determine HW & SW Requirements

Develop or Acquire User IP

SW Design
- Develop/Edit SW Program
- C Compile
- SW Simulation & Debug

Fail
- Circuit Synthesis
- Behavioral Simulation
- Edit Sub-Block IP & Testbench
- Back-Assertate
- Timing Driven Simulation
- Layout
- Compile
- Encrypted Bitstream/STAPL

Pass
- HW Design

Program SW to FPGA Device
- SW Debug & Verification
- Program FPGA Device HW

Fail
- Design Complete
- Design
- Program FPGA Device
- SW Debug & Verification
- Program SW to FPGA Device
- Development Board

Design Complete

5th Int. Forum on Application-Specific MPSoC © 2005 Actel Confidential and Proprietary July '05
Summary

- We are in a unique position to integrate multi-mode silicon – analog, flash, logic/FPGA, MCU
- Fusion stack provides a flexible and structured means of utilizing these features
- Fusion tools provide an easy-to-use graphical interface to simplify development
- Fusion opens exciting new capabilities to deliver MPSoC’s