An H.264/AVC Main Profile Video Decoder Accelerator in a Multimedia SOC Platform

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Main Points

• Hardwired design has excellent area, performance, power advantages
• If it is to be used by 1B people everyday, every bit and every cycle count
• It is not difficult
  – 15 CS student-years, no background in video nor HDL-based design; neither is the professor
  – RTL design is the easy part;
  – Understanding algorithm and designing architecture are most critical
# Video Coding Standards

<table>
<thead>
<tr>
<th>Standard</th>
<th>MPEG-1</th>
<th>MPEG-2</th>
<th>MPEG-4</th>
<th>H.264</th>
</tr>
</thead>
<tbody>
<tr>
<td>MB size</td>
<td>16*16</td>
<td>16*16(frame)</td>
<td>16*16</td>
<td>16*16</td>
</tr>
<tr>
<td>Block size</td>
<td>8*8</td>
<td>8*8</td>
<td>16<em>16, 8</em>8</td>
<td>16<em>16, 16</em>8, 8<em>16, 8</em>8, 8<em>4, 4</em>8, 4*4</td>
</tr>
<tr>
<td>Transform</td>
<td>DCT</td>
<td>DCT</td>
<td>DCT/ Wavelet</td>
<td>4*4 int transform</td>
</tr>
<tr>
<td>Entropy coding</td>
<td>VLC</td>
<td>VLC</td>
<td>VLC</td>
<td>VLC, CAVLC and CABAC</td>
</tr>
<tr>
<td>ME, MC</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>41 MVs per MB</td>
</tr>
<tr>
<td>Pixel accuracy</td>
<td>½ pel</td>
<td>½ pel</td>
<td>¼ pel</td>
<td>¼ pel</td>
</tr>
<tr>
<td>Reference frames</td>
<td>One frame</td>
<td>One frame</td>
<td>One frame</td>
<td>Multiple (5) frames</td>
</tr>
<tr>
<td>Picture type</td>
<td>I, P, B</td>
<td>I, P, B</td>
<td>I, P, B</td>
<td>I, P, B</td>
</tr>
<tr>
<td>Transmission rate</td>
<td>Up to 1.5 Mbps</td>
<td>2-15 Mbps</td>
<td>64kbps~2Mbps</td>
<td>64kbps ~ 150Mbps</td>
</tr>
</tbody>
</table>
Get More for Less
H.264/AVC Profiles

Extended profile
- SP, SI slice
- Data partition
- Slice group
- ASO
- Redundant Slice
- B slice
- Weighted prediction
- CAVLC
- Interlace
- CABAC
- 8x8 transform
- Quantization matrix
- Color Sampling
- 8/10/12 bit sampling

Main profile
- I slice
- P slice

Baseline profile
- FREext (High) profile

YLLIN NTHU-CS
NTHU H.264/AVC Main Profile Video Decoder Prototype

Multimedia SOC Platform

FPGA @ 10MHz
Main Profile
CIF(352x288)@ 30 fps

FPGA @ 24MHz
Main Profile
D1 (720x480)@30fps
A Multimedia SOC Platform

- CPU
- Accelerator (FPGA)
- USB (PHY) Daughter Board
- ROM/Flash Memory SRAM
- SDRAM
- VIC
- USB 2.0
- Static memory
- SDRAM Controller (4-CH)
- FPGA
- High-Speed Bus
- JPEG Codec
- DMA
- SRAM
- PWM
- WDT
- TIMER
- APB Bridge
- Capture
- Display Controller
- DAI
- SSI
- SD
- SM
- UART
- GPIO
- 12C
- Audio Codec I2S
- Flash memory with SSI
- Flash Card
- Button
- LED
- Video-In CCIR601
- TV/LCD
H.264/AVC Decoder System Diagram
H.264/AVC Decoder Architecture
Hierarchical FSM in Main Controller

Main controller

Type decoder

Frame Level

MB Level

CABAC FSM

MC FSM

IPRED FSM

IQ/IDCT FSM

PICREC FSM

DF FSM

CABAC

MC

IPRED

IQ/IDCT

PICREC

DF

rden

rd_addr

rd_data

Main FSM
Our Design Flow

1. User Spec.
   - Platform spec.
     - System configuration
   - System description

2. Embedded Software
   - Compilation
     - Software spec. in C & Acceleration specify
     - System.h

3. System Generation
   - API
     - HW lib.
     - System.v
   - Integration
     - Hardware image
   - Pin assignment & Hardware compilation
     - System Integrate
     - System generation

4. Evaluation
   - HW/SW co-simulation
     - Area & Timing & Power evaluation
     - No Performance constraint
     - Yes
   - FPGA prototyping

5. Co-Sim
   - HW lib.
     - HDL IPs
   - Acceleration
     - HW IP Synthesizer
   - Accelerator.v

6. FPGA Verify
   - Platform model
     - Yes
   - Performance constraint
Memory Traffic Consideration

- One SDRAM for All External Storage
- SDRAM Burst Mode
- Internal Storage for Compact Access & Data Reuse

SDRAM
- Encoded Bitstream
- Reference Frames
- Currently Reconstructed Frame
- Display Buffer
Buffer Size vs Bus Traffic

![Graph showing Buffer Size vs Bus Traffic for different frequencies and display types.](image)

- **16MHz/TV**
- **16MHz/LCD**
- **24MHz/TV**
- **24MHz/LCD**

Frame per Sec vs Buffer Size
Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th>DSP Core</th>
<th>HW Accelerated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Count</td>
<td>230K</td>
<td>180K</td>
</tr>
<tr>
<td>MHz</td>
<td>200</td>
<td>10</td>
</tr>
<tr>
<td>Profile</td>
<td>Baseline</td>
<td>Main</td>
</tr>
<tr>
<td>Resolution</td>
<td>QCIF (176x144)</td>
<td>CIF (352x288)</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>15</td>
<td>30</td>
</tr>
</tbody>
</table>
Summary

• An H.264/AVC main profile decoder on an ad hoc multimedia SOC platform
• Hardware-accelerated approach is high-performance and energy-efficient
• Memory traffic has major impact on performance
• It is not as difficult as you may think; algorithm and architecture are critical; writing Verilog is no difference from writing C
• Do not try to parallelize Reference Software; it is just proof of concept; not an implementation
Demo Video