Ultra-Low Power?
Think Multi-ASIP SoC!

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Ultra-low power SoC design

ITRS Roadmap

Table 6b  Power Supply and Power Dissipation—Long-term Years

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2010</th>
<th>2012</th>
<th>2013</th>
<th>2015</th>
<th>2016</th>
<th>2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Node</td>
<td>6P45</td>
<td>6P32</td>
<td>6P22</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRAM ½ Pitch (nm)</td>
<td>45</td>
<td>35</td>
<td>32</td>
<td>25</td>
<td>22</td>
<td>18</td>
</tr>
<tr>
<td>MPU/ASIC Metal 1 (M1) ½ Pitch (nm)</td>
<td>54</td>
<td>42</td>
<td>38</td>
<td>30</td>
<td>27</td>
<td>21</td>
</tr>
<tr>
<td>MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)</td>
<td>45</td>
<td>35</td>
<td>32</td>
<td>25</td>
<td>22</td>
<td>18</td>
</tr>
<tr>
<td>MPU Printed Gate Length (nm) ††</td>
<td>25</td>
<td>20</td>
<td>18</td>
<td>14</td>
<td>13</td>
<td>10</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>18</td>
<td>14</td>
<td>13</td>
<td>10</td>
<td>9</td>
<td>7</td>
</tr>
<tr>
<td>Power Supply Voltage (V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vdd (high-performance)</td>
<td>1.0</td>
<td>0.9</td>
<td>0.9</td>
<td>0.8</td>
<td>0.8</td>
<td>0.7</td>
</tr>
<tr>
<td>Vdd (Low Operating Power, high Vdd transistors)</td>
<td>0.7</td>
<td>0.7</td>
<td>0.6</td>
<td>0.6</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Allowable Maximum Power [1]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-performance with heatsink (W)</td>
<td>218</td>
<td>240</td>
<td>261</td>
<td>270</td>
<td>288</td>
<td>300</td>
</tr>
<tr>
<td>Cost-performance (W)</td>
<td>120</td>
<td>131</td>
<td>138</td>
<td>148</td>
<td>158</td>
<td>168</td>
</tr>
<tr>
<td>Battery (W)—(hand-held)</td>
<td>2.8</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
</tr>
</tbody>
</table>

[1] Power will be limited more by system level cooling and test constraints than packaging

- Power budget (Watts) more or less constant, while chip complexity increases
Ultra-low power SoC design

**Dynamic power**

\[ P_{dyn} = C \times (A \times f_{clock}) \times V_{dd}^2 \]

- Low-voltage technology, voltage scaling
- Concurrency: task-, data-, instruction-level parallelism
- Avoid unnecessary switching: clock gating, operand isolation...

**Leakage power**

\[ P_{leak} = I_{leak} \times V_{dd} \sim (a^{-vt} \times N_{gates} \times W_{dev}) \times V_{dd} \]

- Multi-threshold cell libraries
- Power gating
- Minimal logic (application-specific)

Ultra-low power SoC design

Holistic approach

- **Holistic adj**
  
  “Emphasising the importance of the whole and the interdependence of its parts”

- Design phases considered
  - System architecture
  - Processor (ASIP) architecture
  - Logic level
System architecture

System-on-Chip becomes Sea-of-Cores

Homogeneous, multi general-purpose processors
- VLIW/SIMD: NXP (EVP), Sandbridge, Atmel (Diopsis)…
- Array processor: Morpho, IMEC…
- Processor arrays: PicoChip, Cradle…

Heterogeneous, multi-ASIP
- Configurable IP vendors: Tensilica, ARC, SiliconHive…
- EDA vendors: Target, CoWare, ASIP Solutions…

Heterogeneous best for deep submicron power challenge!
- Each ASIP optimised for its function: minimal logic, balanced parallelism
- Well suited for power gating based on system requirements
System architecture

Example: Gennum’s Voyageur platform

- Used in hearing instruments and Bluetooth headsets
- Processor cores designed with Target’s tool suite
  - Multi-core
    - Microprocessor core
    - 4 “μ DSP” VLIW cores
    - 4 filter accelerators
  - 0.04 mW/M-MAC, 42 MIPS at $f_{\text{clock}} = 2 \text{ MHz}$ (0.13μ CMOS)

Courtesy of Gennum Corporation
ASIP architecture

- **Concurrency**
  - Instr.-level parallelism (VLIW or encoded)
  - Data-level parallelism (SIMD)

- **Reduced memory access**
  - Memory hierarchy: data & instr. caches, loop buffer
  - Distributed reg. architecture
  - Encoded instruction set

- **Arch. specialisation**
  - App.-specific data types
  - App.-specific functional units and instructions
  - Balanced pipeline

→ Optimise beyond the limitations of configurable processor templates!
ASIP architecture

True architectural exploration enabled by retargetable tool suite – “Chess/Checkers”

- Optimisation beyond reconfigurable processor templates
- Fast path to logic synthesis allows for accurate power estimations
**ASIP architecture**

**Example: Gennum’s Voyageur platform**

- 0.04 mW/M-MAC, 42 MIPS at $f_{\text{clock}} = 2$ MHz (0.13μ CMOS)
- μ DSP and filter engines: 20-bit precision
- μ DSP: VLIW with dual MAC
- Filter accelerators: same algorithm consumes 4x less power than on μ DSP

Courtesy of Gennum Corporation
Logic level

HDL generator adds logic to avoid unnecessary switching

- Selective clock gating
- Selective operand isolation
- Latching of register file addresses in instruction decoder

Example: audio DSP (90 nm technology, 200 MHz)

<table>
<thead>
<tr>
<th>Design step</th>
<th>Power</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Go - Without low power options</td>
<td>91 µW/MHz</td>
<td></td>
</tr>
<tr>
<td>Go - Clock gating and operand isolation for FUs</td>
<td>57 µW/MHz</td>
<td>(-37%)</td>
</tr>
<tr>
<td>Go - Operand isolation for muxes</td>
<td>44 µW/MHz</td>
<td>(-23%)</td>
</tr>
<tr>
<td>Go - Register addresses from decoder</td>
<td>36 µW/MHz</td>
<td>(-18%)</td>
</tr>
</tbody>
</table>
| Manual HDL design by low-power specialist       | 32 µW/MHz| (-11%)   | 36.6 kGates| (-1%)
Conclusions

- Heterogeneous multi-ASIP SoCs best meet deep-submicron power challenge
  - Optimally balanced task / data / instruction-level parallelism → reduce dynamic power
  - Minimal logic, power gating → reduce leakage power

- Key is retargetable tool suite for efficient ASIP design
  - Enables true architectural exploration, beyond configurable processor templates
  - Provides unified and efficient software development environment

- Fast and efficient path to logic implementation
  - Includes logic-level power optimisations
  - Enables fast and accurate power estimations