Normally-Off Computing for Smart City Applications

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What is Normally-Off Computing?

- Normally-Off (N-Off): aggressively powers off components of computer systems when they need not to operate, even under computation.
- Computing which realizes the ‘Normally-Off’

Key Technology
- Non-Volatile Memory (MRAM, FeRAM, etc.)
- Intelligent Power Management

Strategy:
- not a simple combination of these technologies
- Computing which exploits synergy of these technologies
Introduction of Normally Off Computing Project

- Project supported by NEDO/METI
  - NEDO: New Energy and Industrial Technology Development Organization
  - METI: Ministry of Economy, Trade and Industry
  - Participating Industries: Renesas, Toshiba, Rohm
  - Budget: Half-supported by Government (Approx.) $7M USD / year by NEDO + $7M USD / year by Industry
  - Project Leader: Hiroshi Nakamura (U. Tokyo)

- Update from MPSoC’13
  - Passed intermediate evaluation last year
  - Progress towards Practical Application
Goal of Normally-Off Computing

So Far:

- Combinational logic
- Volatile RAM

Coarse-grained power gating

always ON

- Combinational logic
- Volatile RAM

long time for data save

Non-volatile Storage

Temporally and spatially fine-grained power gating

Power-off area

Power off as much as possible

- Combinational logic (Power Gating)
- Non-volatile RAM

Characteristics of NV-RAM

- Zero Stand-by Power 😊
- Slow speed 😞
- Higher write Power 😞

Ideal

Normally-Off
Importance of Normally-Off: Power Breakdown of Sensor Node

- **Wide Variety:** depends on applications
- **CPU(idle)** is dominant
- **Reduction of CPU Idle Power is important**
  - Environment Monitoring (*)
  - HEMS (Home Energy Management System) [Courtesy of Hayashikoshi@Renesas]
  - HRM (Heart Rate Monitoring) (**)

Challenges of N-Off Computing

- Temporal Granularity
  - Finer Granularity is preferable for Power Reduction

BUT,

- Too frequent power gating increases power consumption
- Too frequent NV-RAM accesses consume larger power consumption
Granularity of Power Management

Available Low Power Mode:
Sleep vs. Deep Stand-by (D-SBY)

- Sleep: Clock Gating, Power Supplied
  - Quick Resume 😊, Small Energy for Resume 😊
  - Waste of Idle Power 😞

- Deep Stand-by: Clock & Power gating
  - Slow Resume 😞, Large Energy for Resume 😞
  - Effective Suppression of Idle Power 😊

Superiority depends on
- Both System and Application Characteristics
Sleep vs. Deep Stand-By

- Parameters: Big Core, Little Core, Sensor & Radio

- Graph showing Daily Energy Consumption (mWh) vs. Sensing Interval (s)
  - Sleep(Big)
  - D-SBY(Big, Tresume=10ms)
  - Sleep(Small)
  - D-SBY(Small, Tresume=1ms)

- Trend lines indicate that energy consumption decreases as the sensing interval increases.

- Big.LITTLE architecture

- Parameters: Big Core, Little Core, Sensor & Radio
**Pitfall**

- Replacing volatile RAM with NV-RAM always leads to power reduction \( \Leftarrow \) *This is FALSE*

- (Important) Access energy
  
  Non-volatile RAM \( > \) Volatile RAM

→ **Break Even Time** of NV-RAM is important

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![Power Consumption of Memory Diagram](image)

- **Break Even Time (BET)**: Time when \( a = b \)
- \( a \): extra access energy
- \( b \): reduced leakage energy
- \( c \): actual reduced energy

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MPSoC’14 (H. Nakamura, U.Tokyo) 2014/7/7
BET of NV-RAM is 1 sec when 1K words are written.

NV-RAM of low access power (=shorter BET) is preferable.
Research Topic (2) “Research on technology to realize innovative normally-off computing for future sustainable social infrastructure”

Central Laboratory

U-Tokyo, Renesas, Toshiba, Rohm

Research Topic (1) “Development of power management techniques by using next generation non-volatile device”

Distributed Laboratory

Topic (1)-1 Mobile Device
Toshiba

Topic (1)-2 Smart City
Renesas

Topic (1)-3 Health Care
Rohm

General Methodology on N-Off Computing

Application Specific Leading-Edge N-Off Computing

THE UNIVERSITY OF TOKYO

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Health Care (ROHM)

ROHM + OMRON HEALTHCARE + Kobe Univ.

- 1st gen. Bio-information sensor
- Image of goal product

<table>
<thead>
<tr>
<th>Measure</th>
<th>Heartbeat, 3-axis acceleration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>22mm*30mm</td>
</tr>
<tr>
<td>Weight</td>
<td>About 4g (w/battery, w/o case)</td>
</tr>
<tr>
<td>Data Transmission</td>
<td>NFC (near field communication) (a.k.a. Wallet Mobile)</td>
</tr>
</tbody>
</table>

Low-power by Normally-Off Computing

Realize wearable measurement by light battery and device

Prevention of lifestyle disease
Block Diagram of ECG Processor

New Algorithm (IHR)

Coretex M0 Core
Normally-Off, 1 wakeup/sec

Data Logging


MPSoc’14 (H. Nakamura, U.Tokyo) 2014/7/7
N-Off Architecture for Low-power Sensor-node (Renesas)

- Sensor-modules are in “Normally-On”.
- Microcontroller is in “Normally-On” or “Intermittent”.

Field Test of Normally-Off Computing

- Demand Transportation System as an IT-assisted convenient public transportation conducted by Renesas Electronics
  - Detection of Demand/User
    - Intelligent Bus Stop
  - Notification of Arrival Time
  - Bus Dispatch
  - Direction to Drivers
  - Test at Nanae Town
    - Area 216.61km²
    - Pop. 28,941
Intelligent Bus Stop

Interface

- High Load
  - Camera
  - Display
  - WiFi
  - ...

- Low Load
  - Pyroelectric sensor
  - Button
  - ...

First Prototype Single CPU
→ Heterogeneous CPUs

Current Time

Bus Dispatched
Expected Arrival Time 10:45
Just departed XX
Concluding Remarks

- Opportunities of Normally-Off Computing
  - Intelligent Power Management
  - Non-volatile memory: Potential is extremely high: fast, large capacity, and low power

- Challenges: Temporal Granularity
  - BET is the most important
  - Optimize memory accesses, core activity to meet BET
  - Optimize architecture to make BET longer
  → Co-Optimization of Algorithm, Software, Architecture and Circuit Design is the KEY

- Status on Smart City Applications
  (by Renesas and ROHM)