System-level Modeling and Validation Solutions for Heterogeneous MP-SoCs

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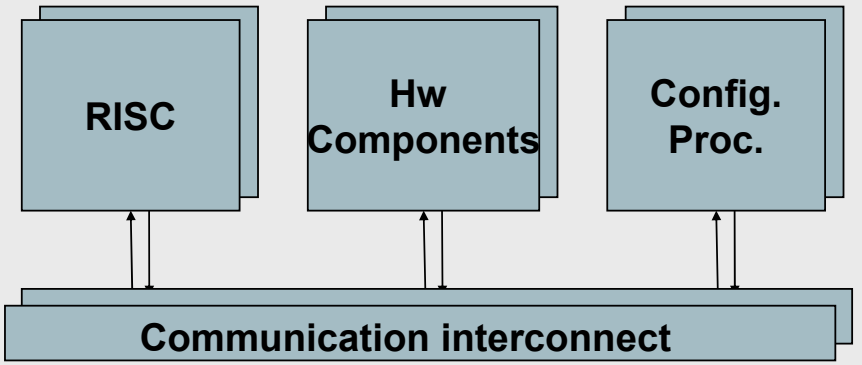
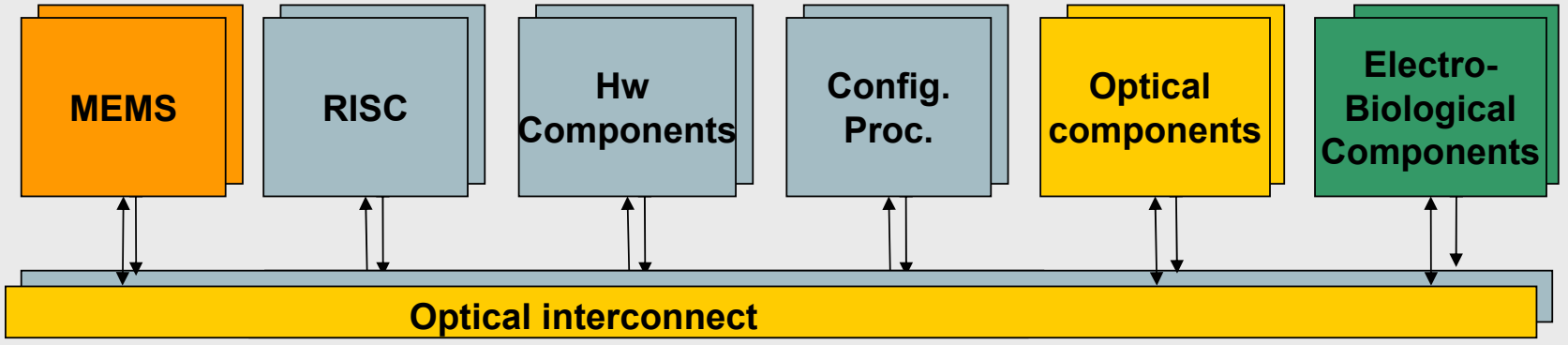
Heterogeneous SoC (1/2)



- Different processors (RISC, configurable processors, …)
- Different hardware components (IPs, Memory,…)
- Different interconnects and communication protocols

Heterogeneous SoC (2/2)

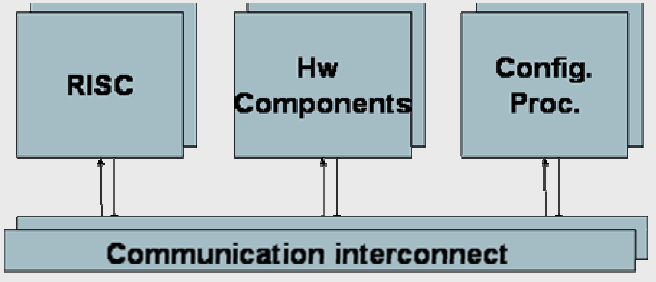


- SoCs are drivers for several technologies integration
  - ITRS 2003 previsions
    - MEMS & Electro-optical components (2004)
    - Electro-biological components (2006)
    - …
- More efficient SoC in the near future
- New CAD tools will be needed

Outline

- Current requirements for MPSoC
- Multi-technology benefits for MPSoCs – example for optical interconnect on chip
- System-level modeling & validation for multi-technology SoCs – challenges and possible solutions
- Conclusion

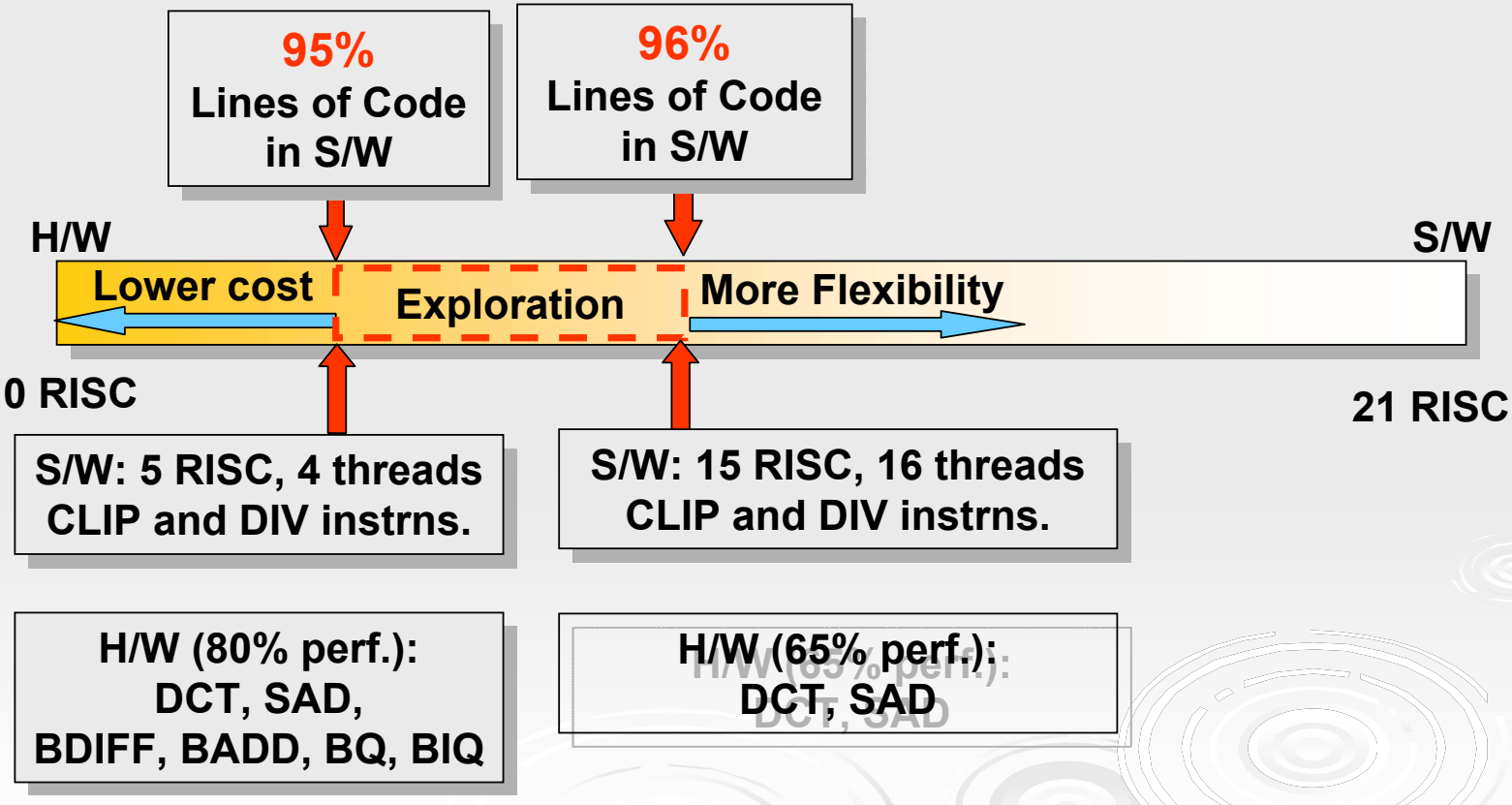
Current MPSoC platforms objectives



- Flexibility & Efficiency
  - Using increasingly Sw for function implementation
  - Parallel processing for low power and scalability
- Fast time-to-market for platform user(s)
  - Need clean programming models
  - Design platform to support programming models
  - Simple, predictable, scaleable SoC interconnect

Example: ST MPEG4 Codec trials

- 30 frame/sec, VGA resolution



Example: ST MPEG4 Codec trials

- 30 frame/sec, VGA resolution
- Design space exploration
  - 5 processor architecture
    - 95% lines of code in S/W
    - 80% performance in H/W
    - Bandwidth: S/W = 1.2 GB/s H/W = 2 GB/s
  - 15 processor architecture
    - 96% lines of code in S/W
    - 65% performance in H/W
    - Bandwidth: S/W = 3.6 GB/s H/W = 1 GB/s

Current Requirements vs. Interconnect Solutions

- Requirements for MPEG4 codec example
  - 5 proc. arch.: S/W = 1.2 GB/s H/W = 2 GB/s
  - 15 proc. arch.: S/W = 3.6 GB/s H/W = 1 GB/s
- 100 processors S/W > 20 GB/s
- Traditional bus
  - 0.8 GB/s at 200 MHz (burst, 100% use)
- Experimental NoCs
  - 3-6 GB/s at 200 MHz (near 100% use)
- Common to all NoC's: Long latency

- Bandwidth and latency represent a real challenge

Interconnect Challenges at 90nm and beyond

- Interconnect delay > gate delay
- Interconnect area >> gate area
- RTL + physical synthesis needed
- Increasing transmission delay
  - at 65 nm: over 5 clock cycles to transmit signal from chip end-to-end
- Deep sub-micron effects
  - crosstalk, voltage isolation, wave reflection, …

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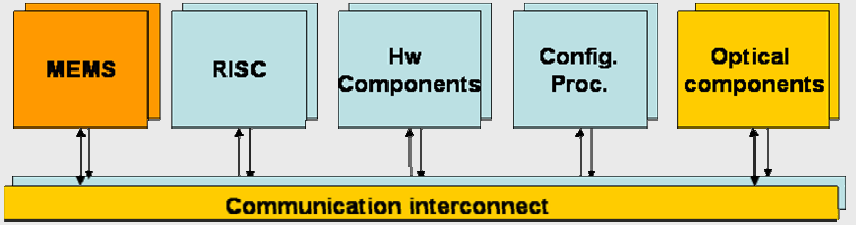
Multi-technology (MT) and MPSoC



- MT may be exploited to overcome the presented challenges for MPSoC
  - Example - optical interconnects in MPSoC
    - High bandwidth and density
    - Reduction of power dissipation
    - Relieve of a broad range of design problems experienced in current electronic systems (crosstalk, voltage isolation, wave reflection, …)
    - Routing congestion problems alleviated

Optical interconnect on chip – reality check –

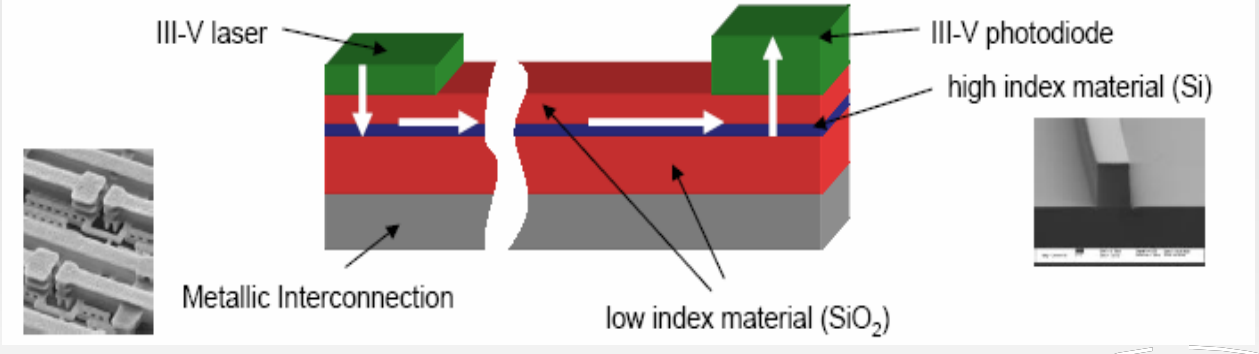
- First results for optics joined with silicon
- Industrial applications
- Possible technological solutions
- Possible MPSoC architecture including optical interconnects

First results for optics combined with silicon

- Stanford university
  - Study showing that several effects (crosstalk, voltage isolation, wave reflection, …) may be relieved by optics
- DARPA, IBM R&D and Agilent technologies
  - New program for development of optical-interconnect chips
- McGill University
  - Study of optical interconnect for very short distances
- IMEC
  - Approach for adding a high density photonic interconnect layer on top of silicon IC's

Possible technological solution

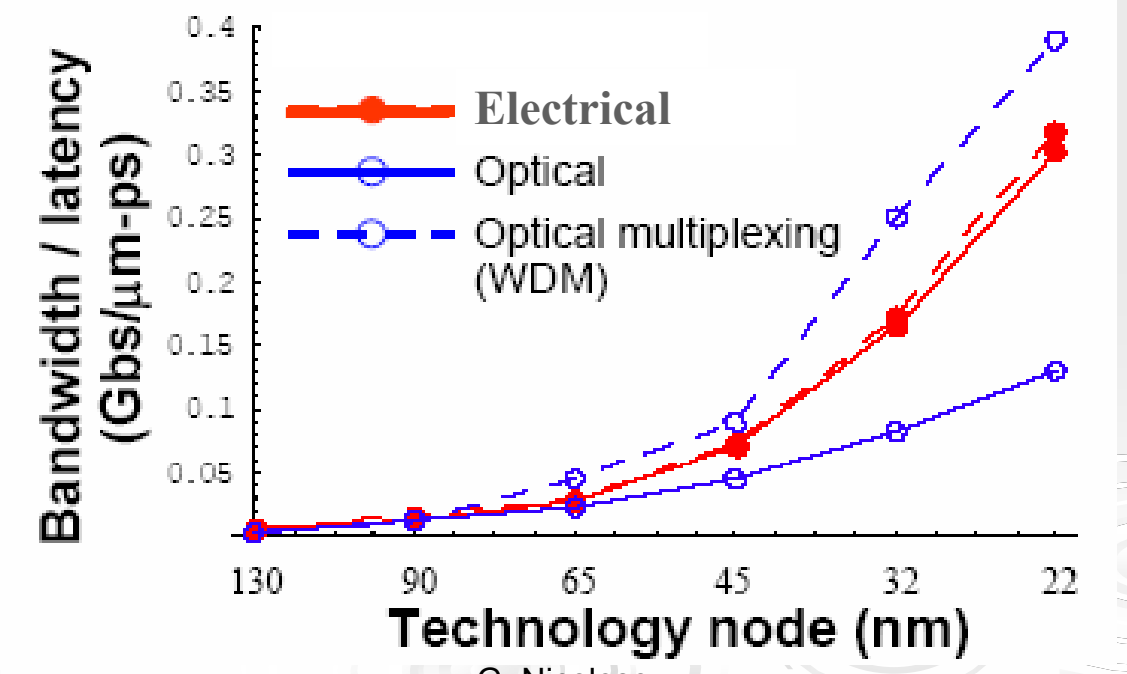
- Optical devices (passives and actives) above the classical integrated circuits
- Compatible with CMOS technology



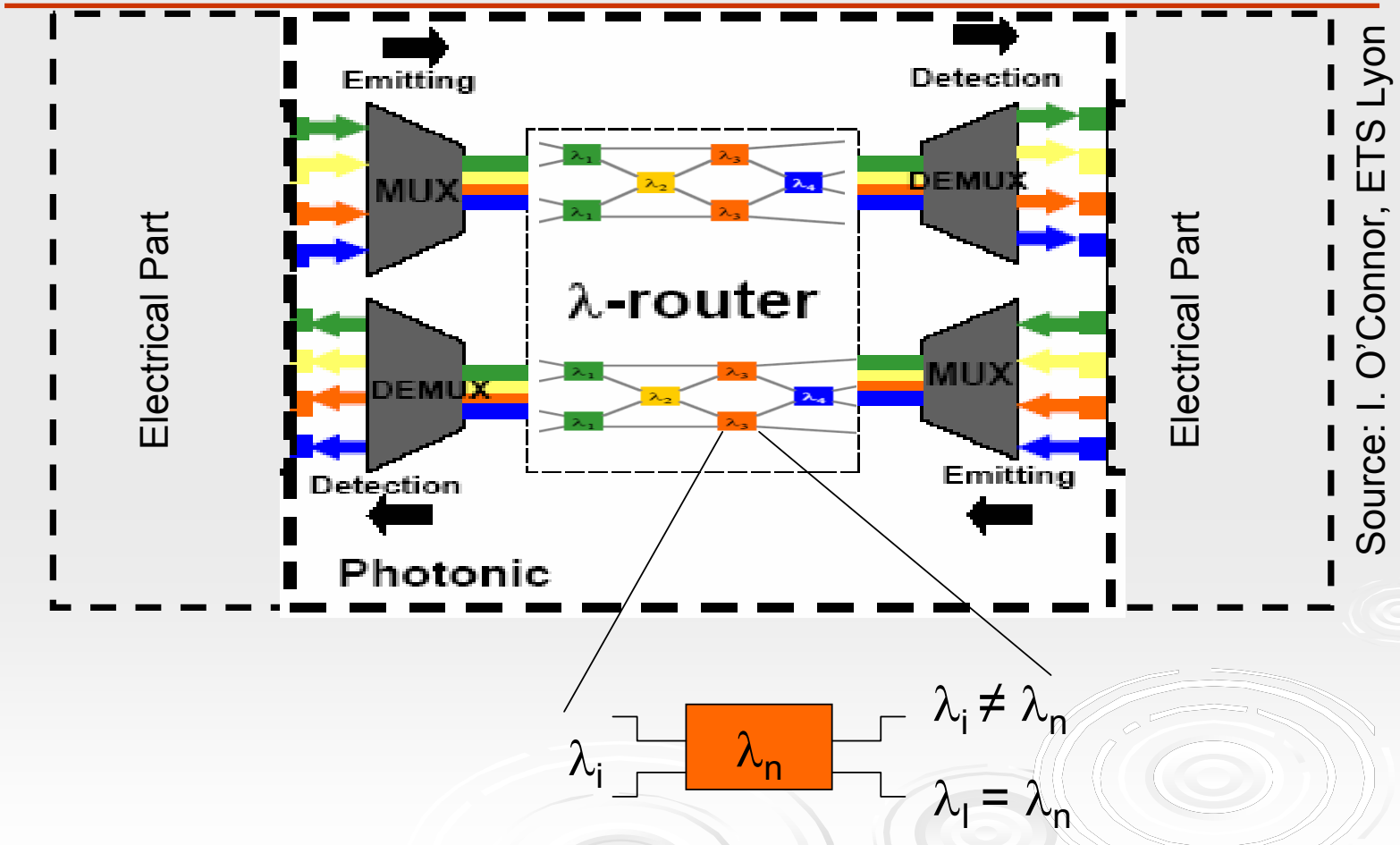
Source: I. O'Connor, LEOM, ETS Lyon

Industrial application

- Technology and Manufacturing Group, Intel Corporation
  - Optical Interconnects on chip provide better bandwidth/latency ratio comparing to classical interconnect



Possible architecture



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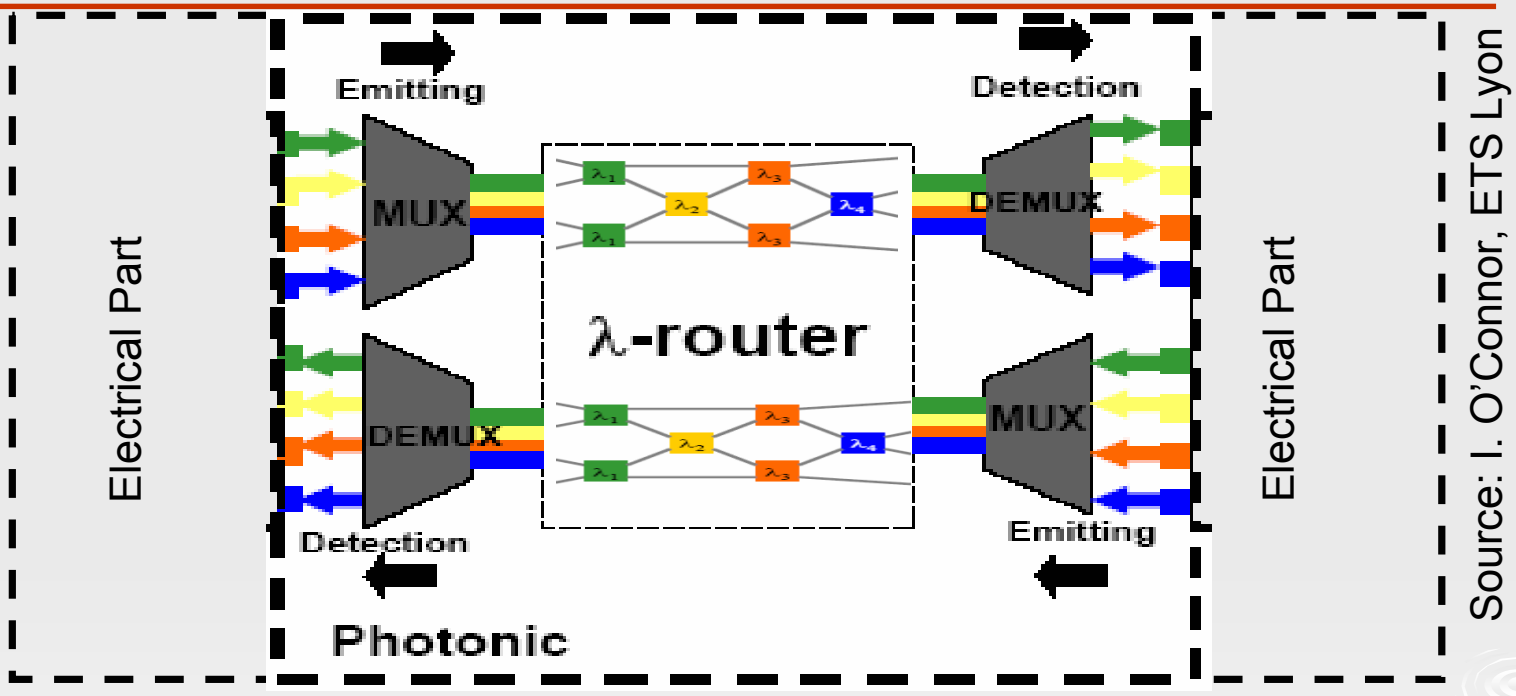

- Multiple signals of dif. wavelengths in the same waveguide
  - no contention, bandwidth density → 20 GB/s
  - simple, scaleable interconnect → simpler prog. models
- 4x4 optical cross-bar - 0.00425 mm^2 for passive network

Outlook for the design of MT-SoC

- Access to physical prototyping for multi-technology SoCs is a major challenge
  - Significant cost
  - Harder to influence standard processes
- Modeling and simulation becomes a necessary alternative in design space exploration for these systems
  - Definition of new CAD tools is mandatory
    - Definition of new specification and execution models
    - The major challenge – accommodating the different application domains (optical, electrical, mechanical)

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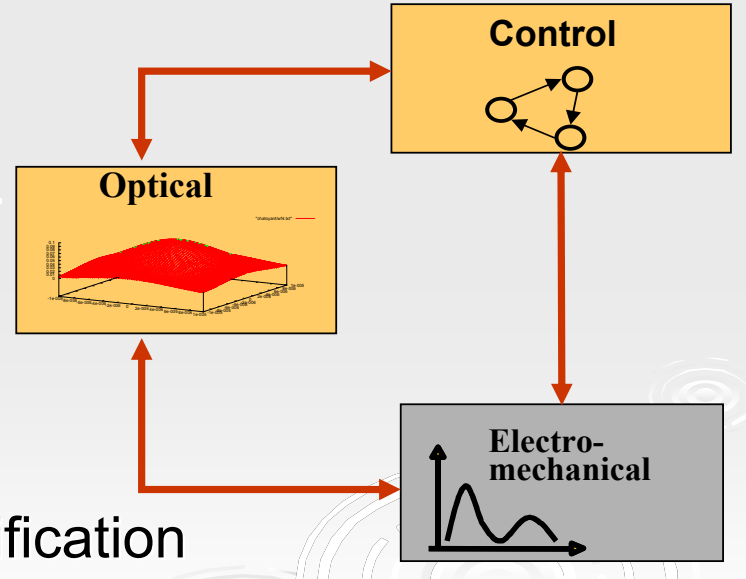
Challenges for MT-SoC Specification & Validation (1/3)

- Heterogeneous components specific to different application domains
  - Diversity of specification & execution solutions
    - Specification languages
    - Abstraction levels
    - Synchronization & comm.



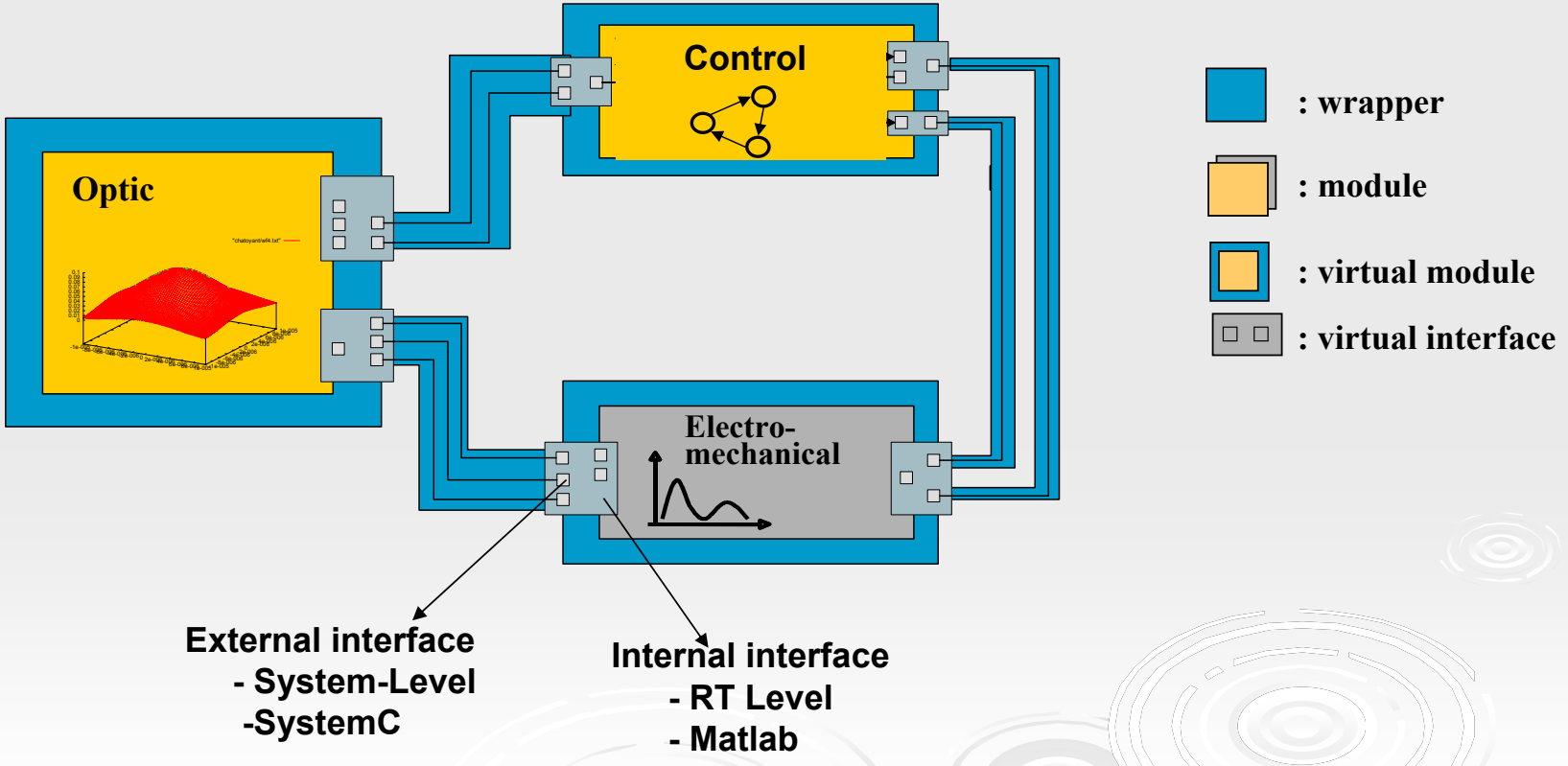
- No ideal solution for global specification
- No ideal solution for global execution

Objective for specification

- Define a new model for global representation of heterogeneous systems
  - Abstract interfaces hiding adaptations required for assembling different components
  - Clear separation between behavior and communication
  - Clear separation between modeling and execution

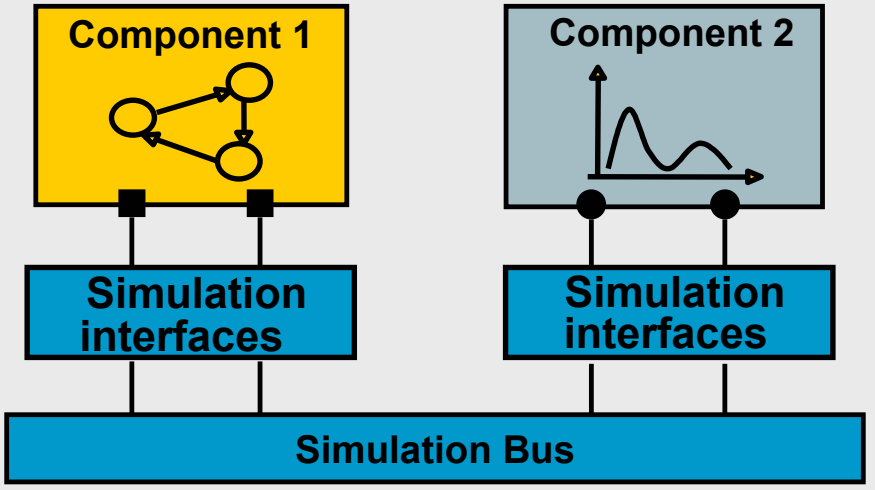
Representation Model for Heterogeneous Systems Specification

Virtual Architecture



Classical Execution Model

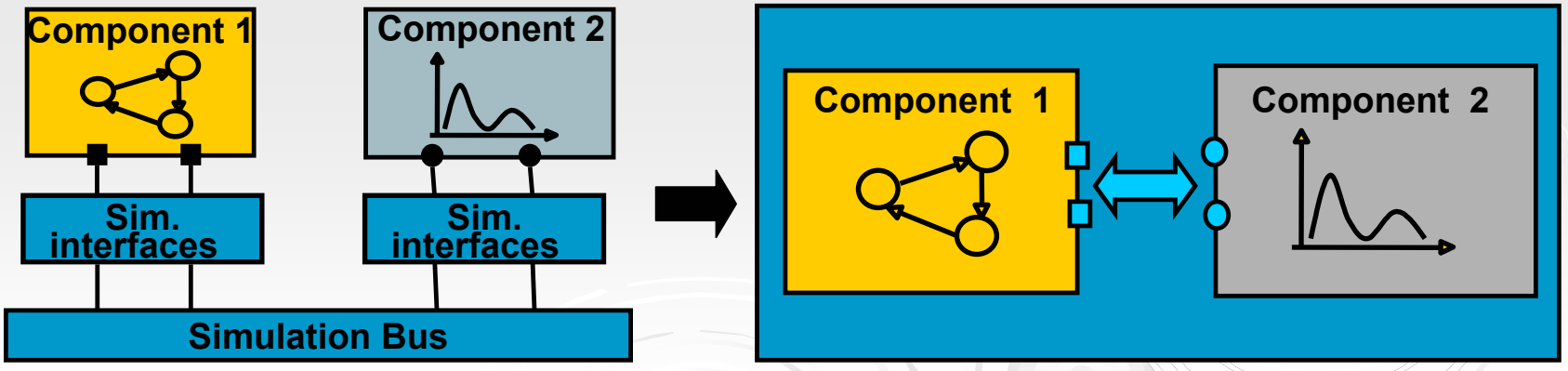
- Component execution models
- Interconnection execution models
- Ad-hoc simulation interfaces
- No automatic composition of heterogeneous components



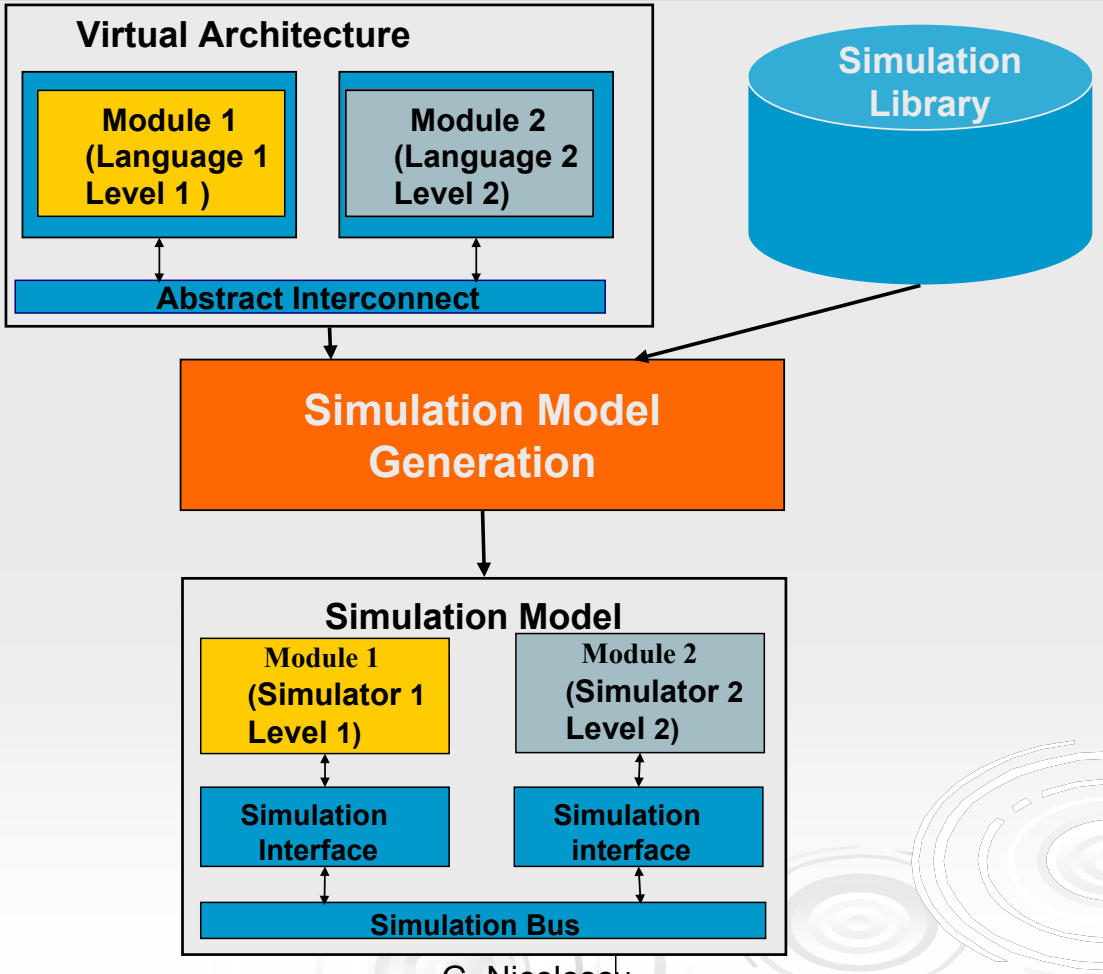
- Building execution models
  - Source of errors
  - Increase the design time

New Approach: Execution Model Abstraction

- Abstract interfaces
- Abstract models for interconnections between heterogeneous components
- Automatic composition of component execution models



First Results: Flow for Automatic Generation of Simulation Models



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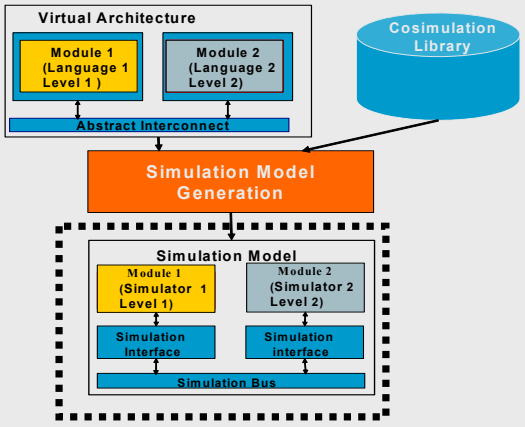
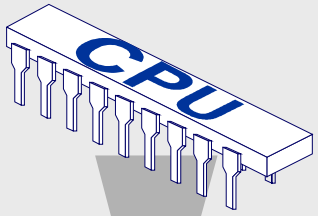
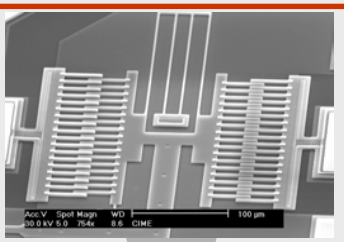
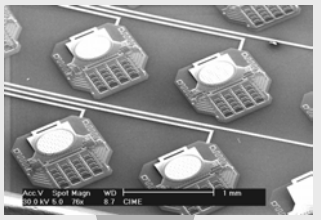


- Simulation interface : execution model of abstract interfaces providing adaptations between
  - Different abstraction levels
  - Different communication protocols
  - Different specification languages
- Simulation bus : interpretation of interconnect at different abstraction levels
  - Abstract
  - Physical
- SystemC - based solution

Specification and validation of an optical switch







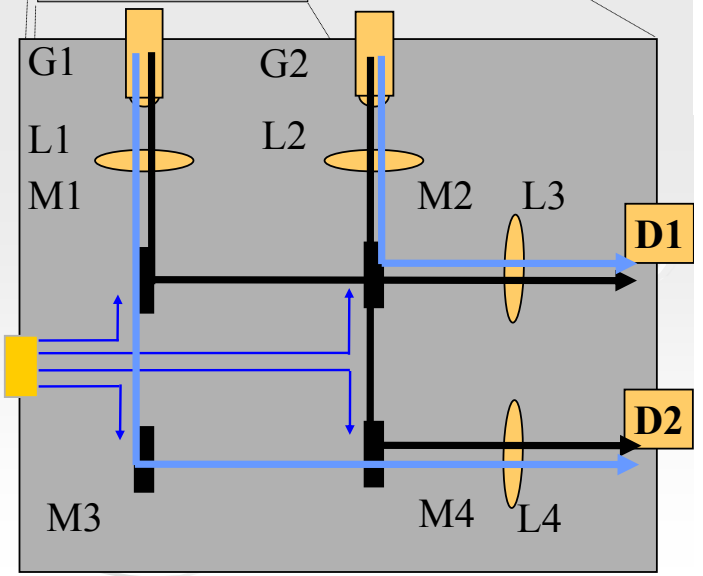
Control Sub-system → **Electro-mechanical Sub-system** → **Optical Sub-system**

Light source

Lens

Mirror

Photo-detector



- Two possible configurations:
  - Mirrors 1 and 4 - reflect light
  - Mirrors 2 and 3 – reflect light

First Result Summary

- Cosimulation environment working
  - Eased cooperation of different teams, different cultures
    - Provided specification model
  - Writing library elements for simulation interfaces generation
    - Integrate Matlab in the cosimulation environment
    - Integrating models of optical devices in SystemC
- Debugging system models
  - Improved functionality when several mirror models joined together into an array
- Debugging overall communication
  - Early and fast global system validation

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Conclusion

- SoC evolution
  - MPSoC architectures with large scale parallelism
  - Multi-technology integration (optical, MEMS, RF, etc.)
- These two trends may be complementary
  - Future heterogeneous MPSoC
    - Optical interconnect integration to overcome interconnect challenges
- Key contribution for heterogeneous MPSoC design
  - New EDA tools accommodating different application domains
    - Global specification models
    - Automatic generation for global simulation models
- Outlook: Global specification and validation for SoC including optical networks
  - More analysis of existing execution models
  - Deeper study of particular simulation interfaces (opto-electric & electro-mechanical)
  - Advanced definition, formalism for simulation interface