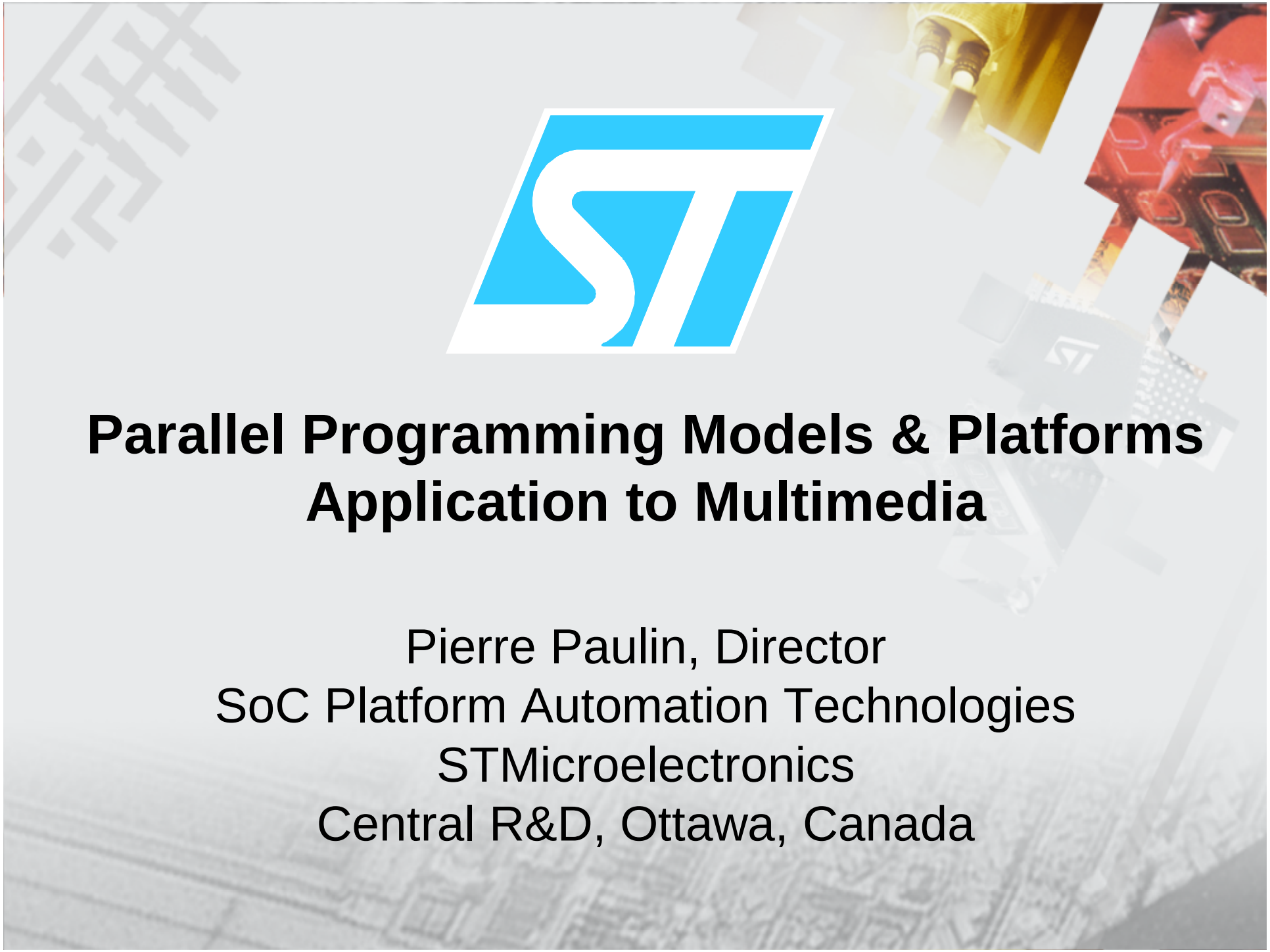
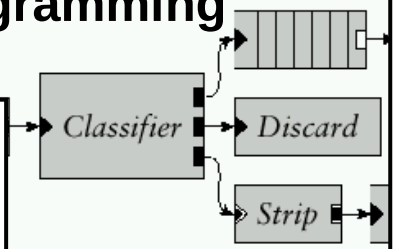


Parallel Programming Models & Platforms
Application to Multimedia

Pierre Paulin, Director
SoC Platform Automation Technologies
STMicroelectronics
Central R&D, Ottawa, Canada

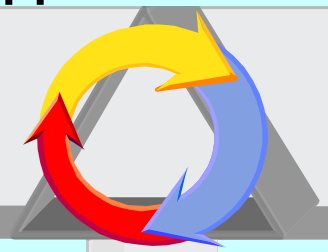
Parallel programming models



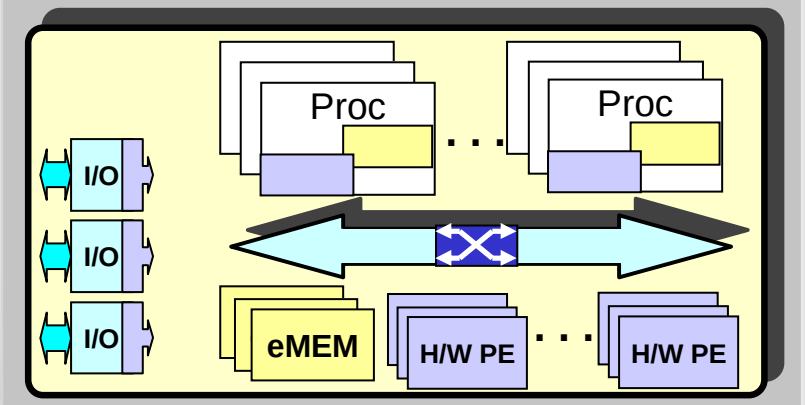
- ✓ Proven, established programming models
- ✓ User-defined parallelism

Application S/W

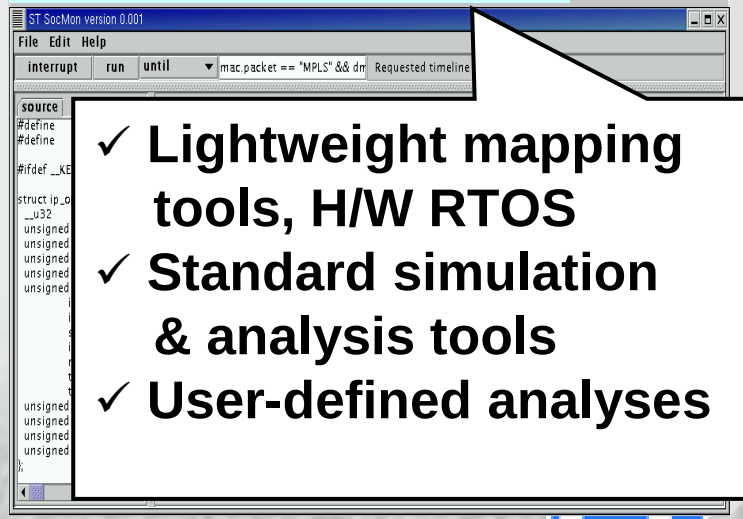
- ✓ Keep it simple, regular, predictable
- ✓ Use industry standards: Processors, NoC, I/O
- ✓ Simplify use of legacy architectures



FlexMP SoC Platform



MultiFlex SoC Tools

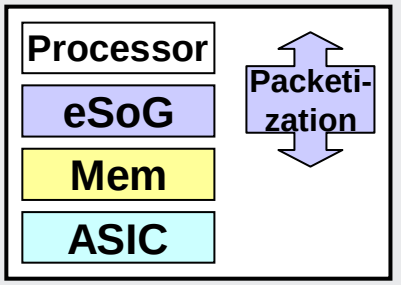


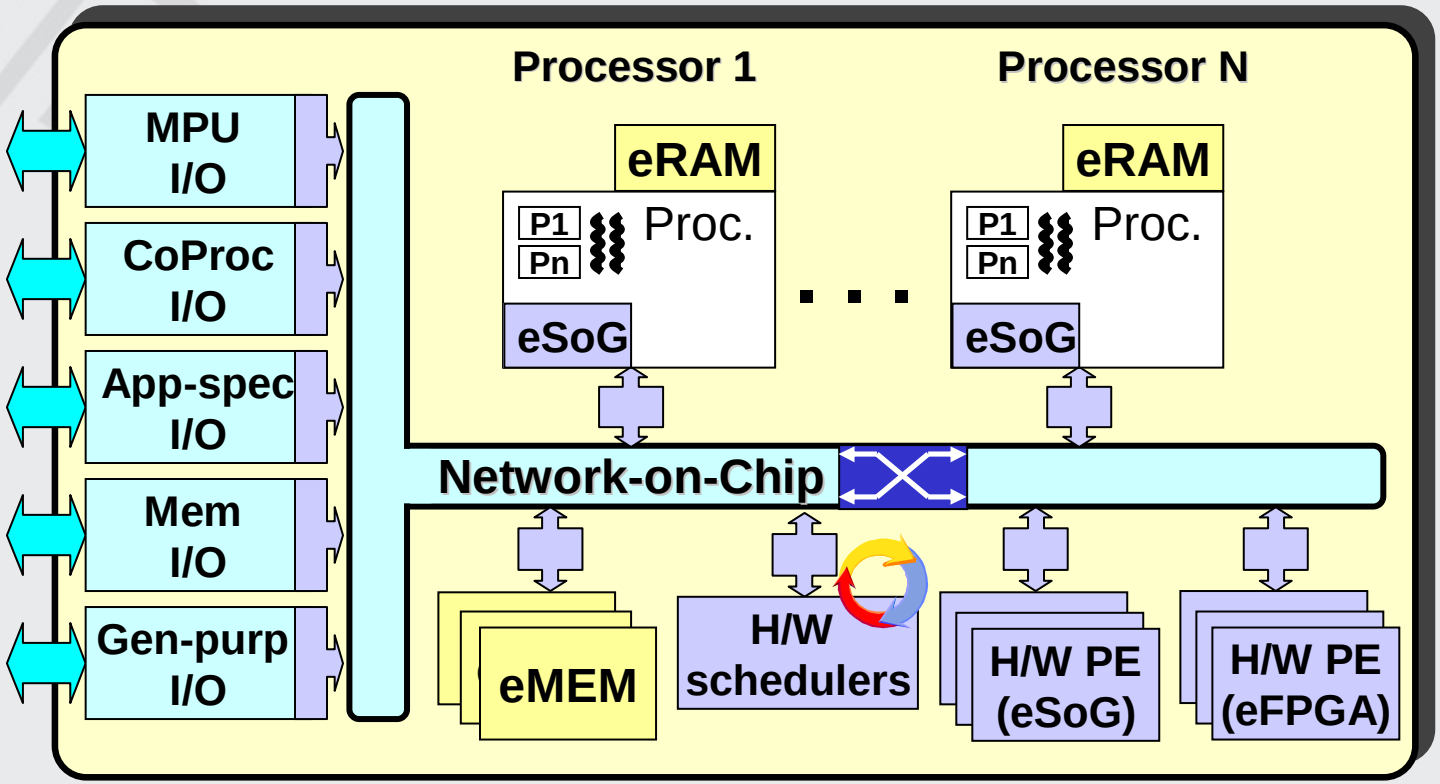
- ✓ Lightweight mapping tools, H/W RTOS
- ✓ Standard simulation & analysis tools
- ✓ User-defined analyses

Outline

- FlexMP architecture platform
- MultiFlex Tools and Methodologies
  - MP-SoC compilation, H/W O/S
- Applications
  - **MPEG4 video codec**
  - 10 Gb/s IPv4 packet forwarding
  - 2.5 Gb/s traffic manager
  - 3G basestation

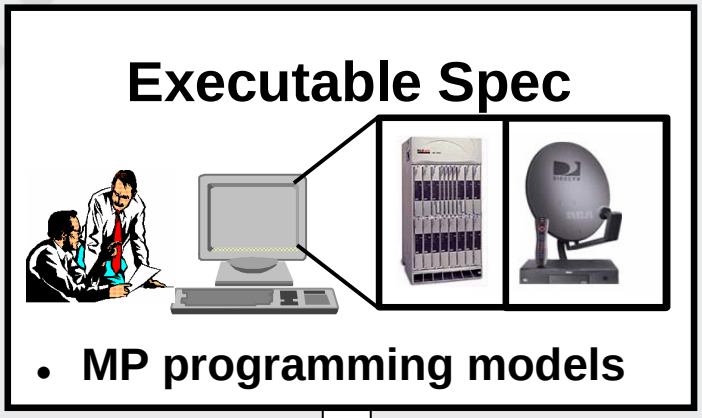
FlexMP SoC Platform





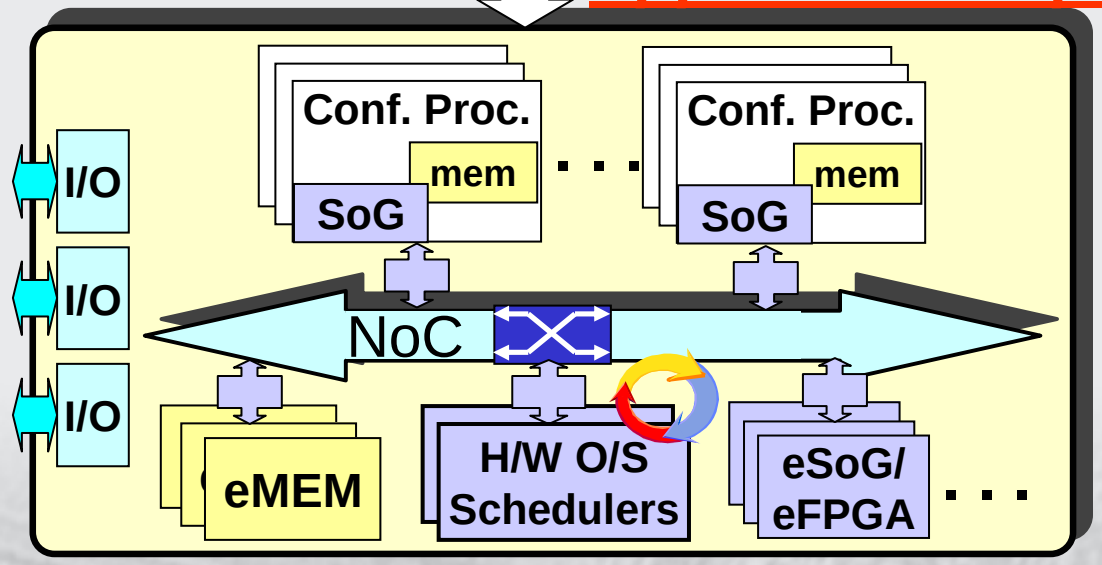
- Multi-threaded, multi-processor platform
- Popular processor models w. config. extensions: H/W multithreading and pipeline depth

MultiFlex MP-SoC Platform Tools



- Two parallel Programming Models
  - DSOC: Message passing
  - SMP: Shared memory

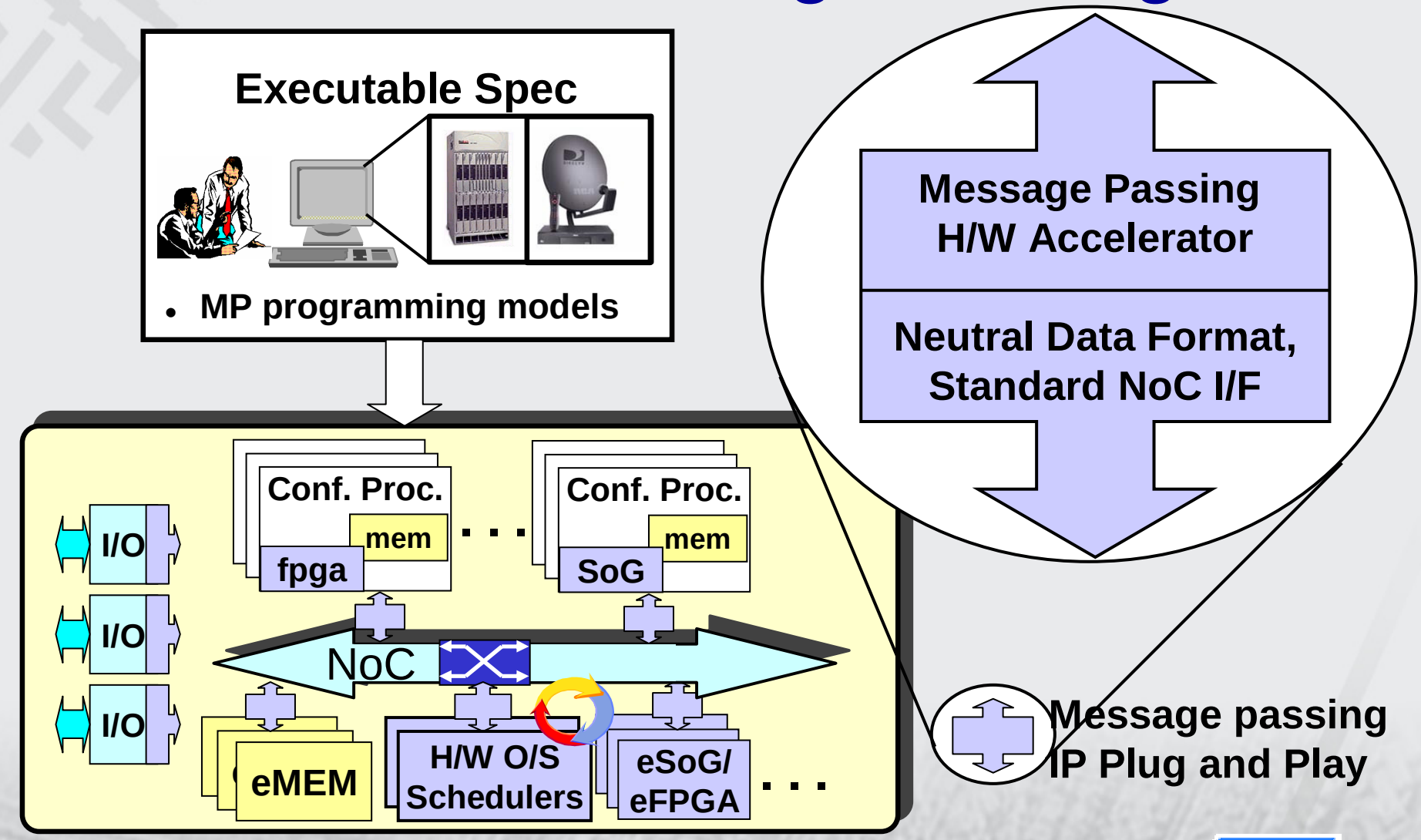
Application to platform mapping



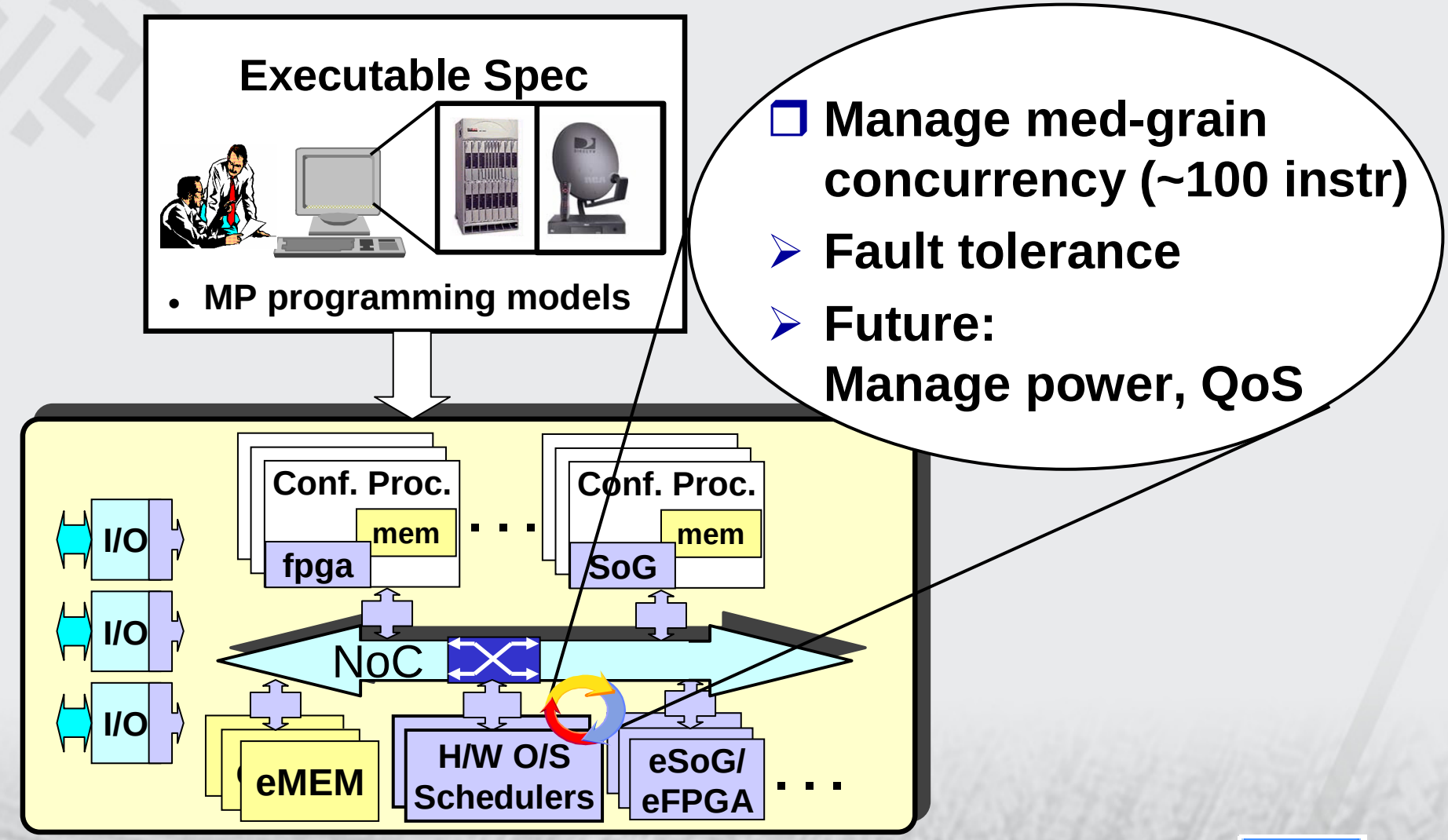
H/W message passing, IP Plug and Play

H/W MP-O/S scheduler accellerators

MultiFlex Message Passing

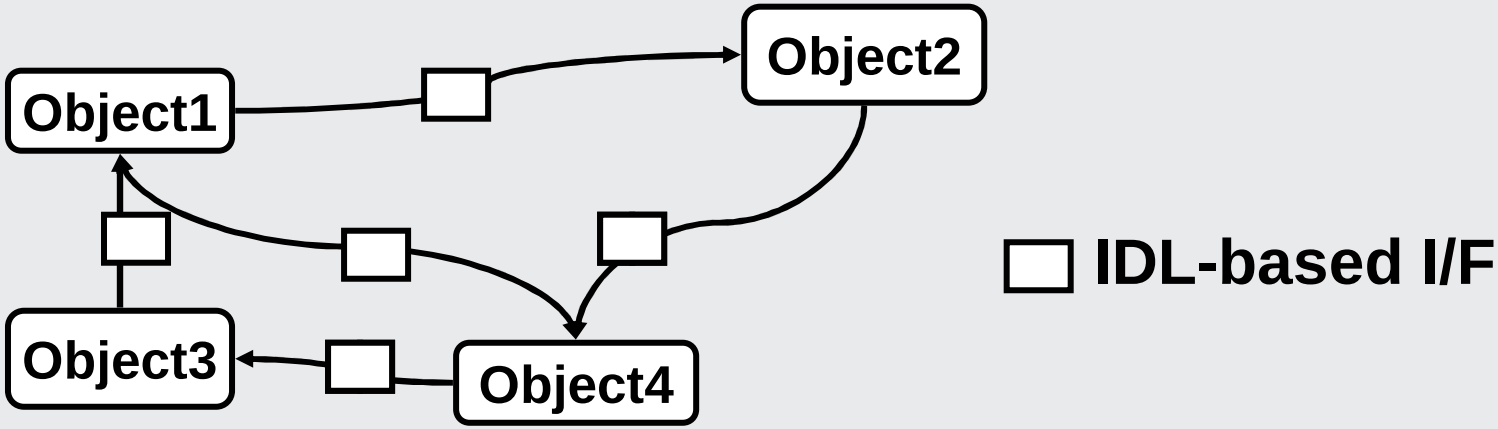


MultiFlex H/W O/S



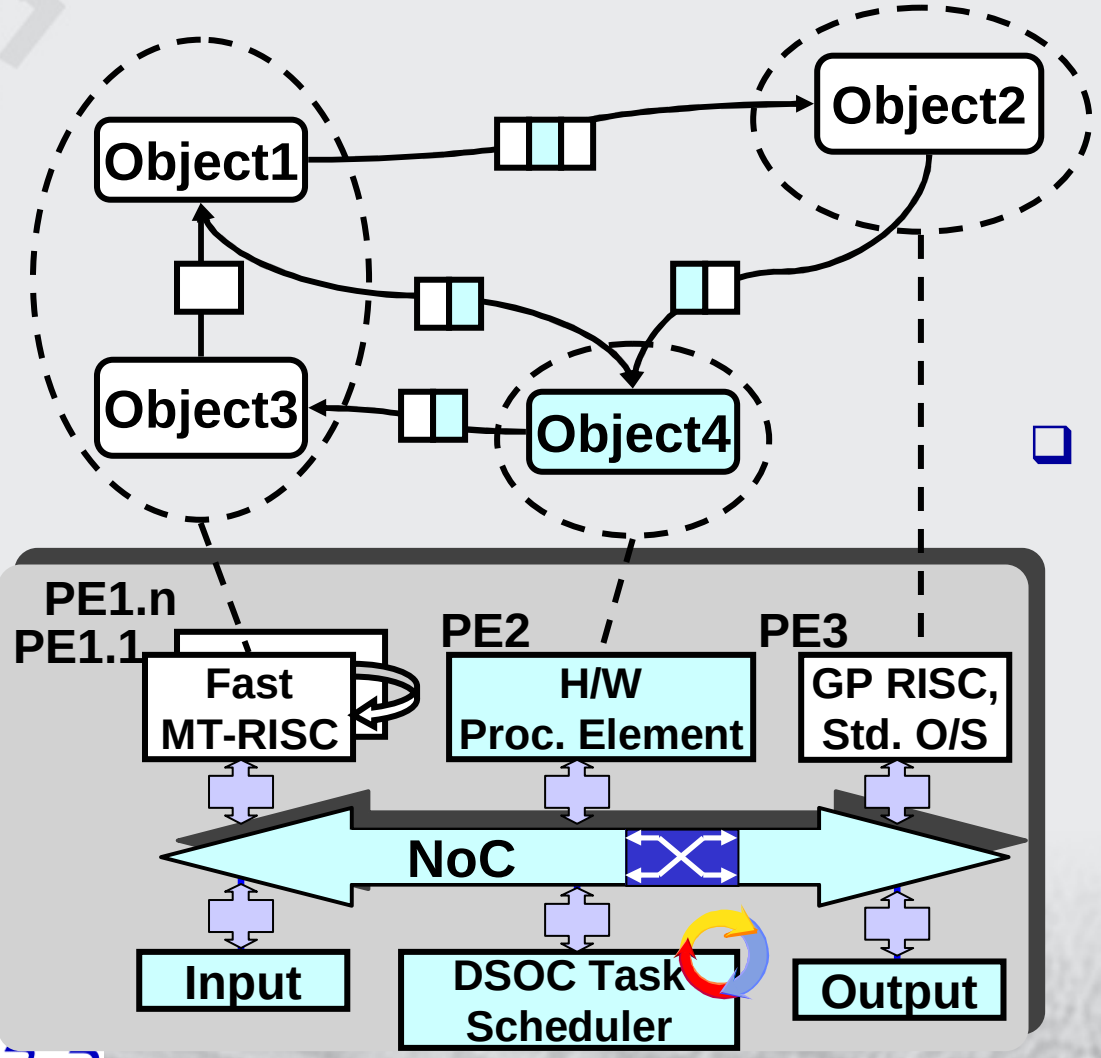
- Manage med-grain concurrency (~100 instr)
- Fault tolerance
- Future: Manage power, QoS

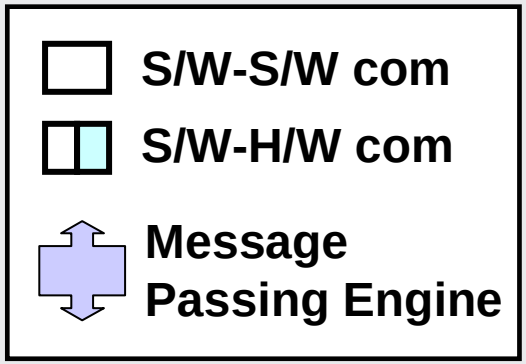
Message Passing Model: DSOC (Distr. System Object Component)



- Based on leading distributed S/W concepts
  - E.g. CORBA, DCOM
- Objects represent application functionality
- Inter-object communication via standard I/F
  - Use of lightweight **I**nterface **D**escription **L**anguage
- Platform independent, no mapping assumptions

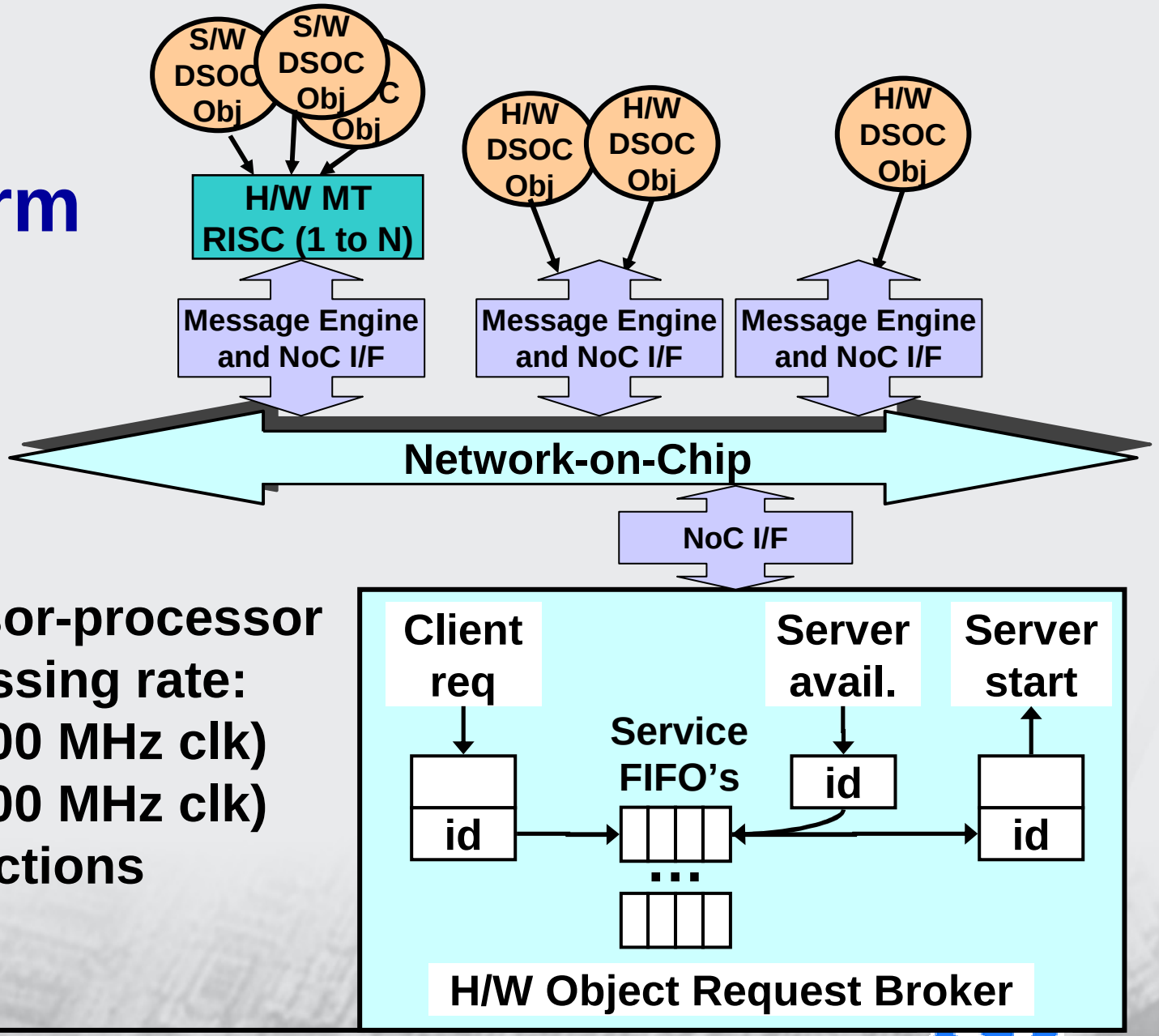
DSOC to Platform Mapping





- Synthesis from IDL: Auto generation of
  - Drivers between different O/S
  - Drivers between S/W PE's and network-on-chip
  - Glue logic between H/W PE's and NoC

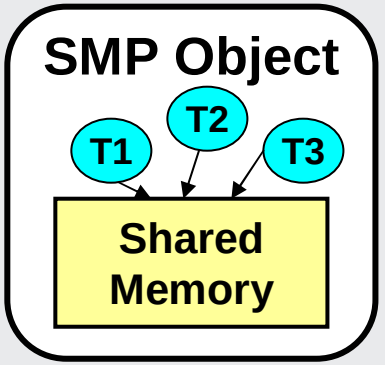
DSOC Platform



Max processor-processor message passing rate:

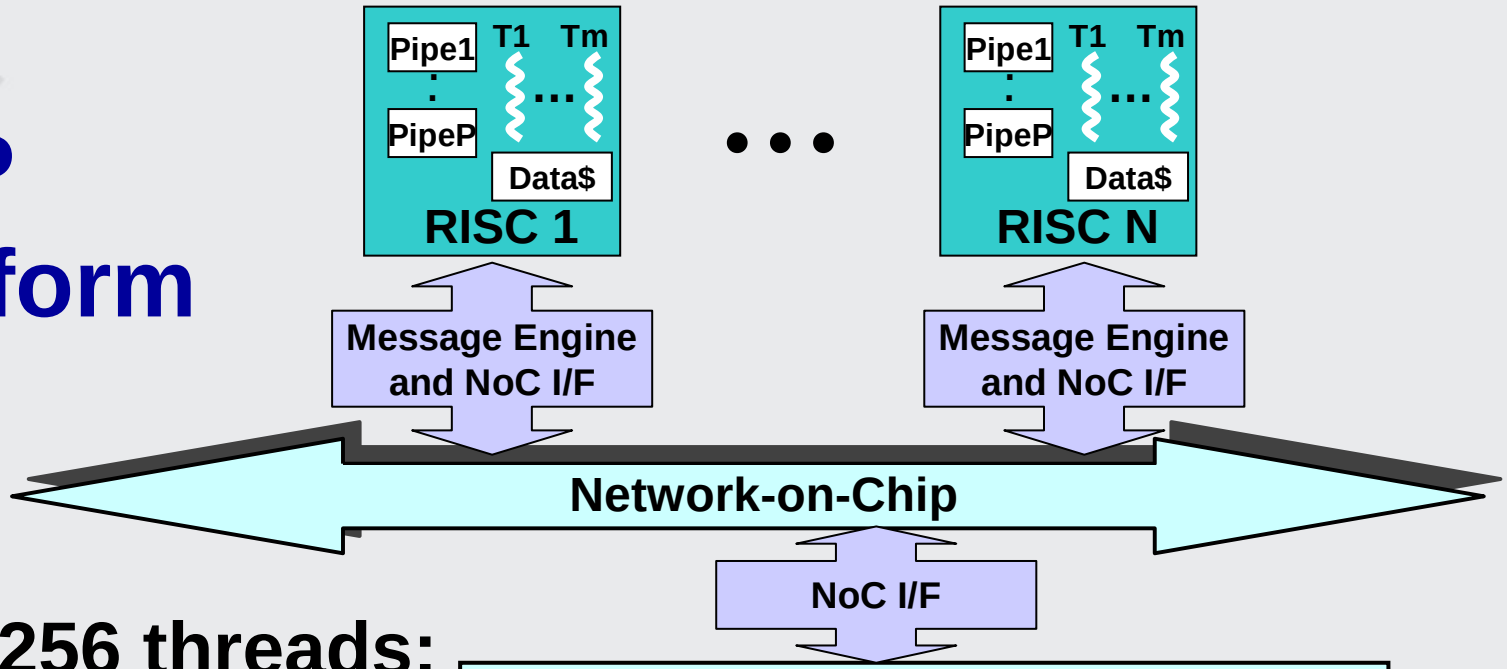
- **35 MHz (500 MHz clk)**
- **15 MHz (200 MHz clk)**
- **<15 instructions**

Programming Model 2: SMP



- Symmetric multi-processing with shared-memory
  - Complement to DSOC programming model
    - ⇨DSOC object may have SMP internal implementation
  - SMP is more natural MP model for Multimedia
- SMP Nano-kernel written in C and C++
  - Java/C# style concurrency primitives implemented with C++ API (or C Posix API)
  - Hardware O/S assists in implementation

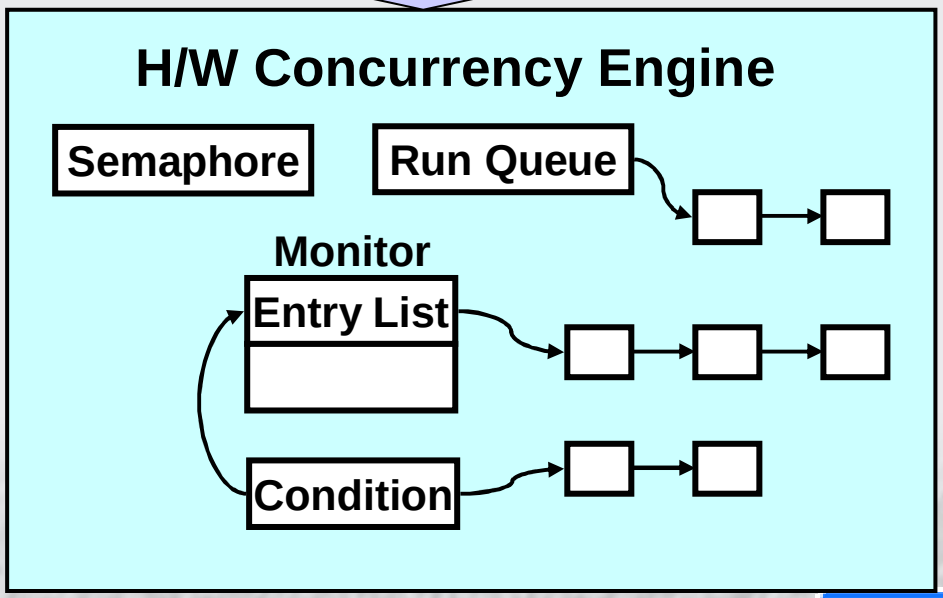
SMP Platform



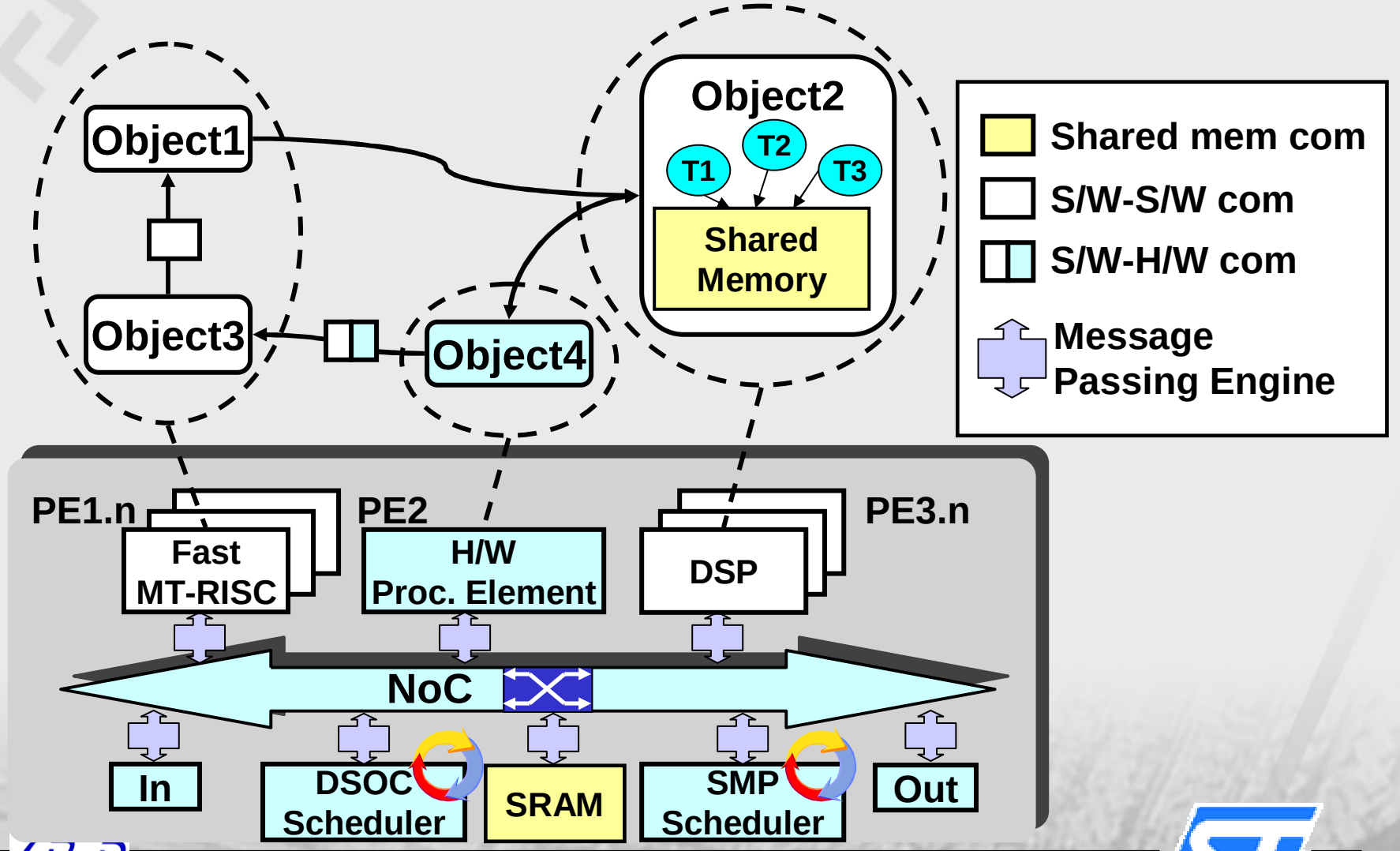
Fork 1~256 threads:

10 instructions (50ns @200MHz)

+ 12 cycles/thread (in conc. engine)



SMP/DSOC to Platform Mapping

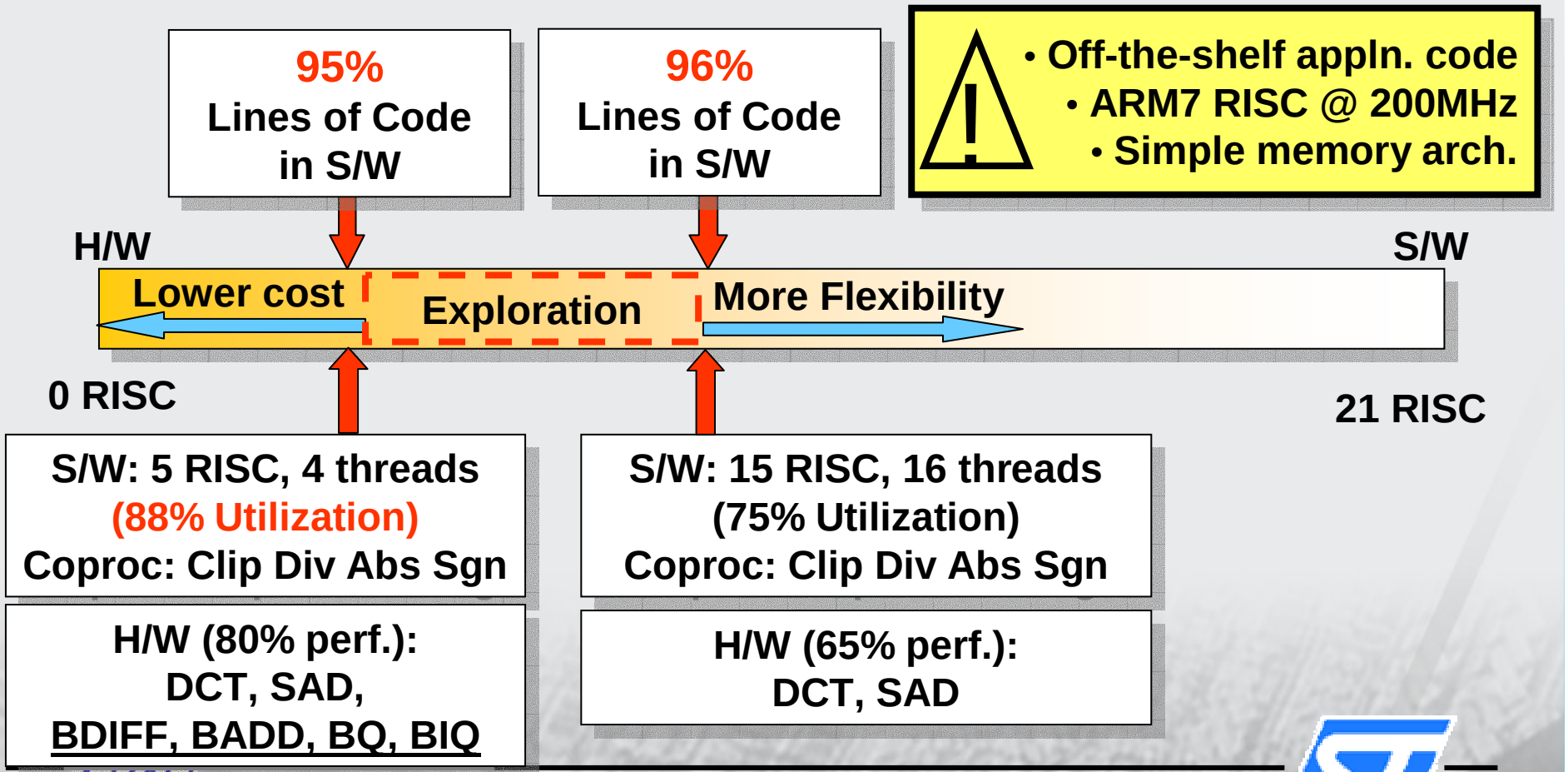


Outline

- *FlexMP* architecture platform
  - Multi-threaded processors, Flexible H/W
  - Network-on-Chip (NoC) interconnect
- MultiFlex Tools and Methodologies
  - Multi-Processor SoC analysis and debug tools
  - MP-SoC compilation, H/W O/S
- ***Applications***
  - ***MPEG4 video codec***
  - 10 Gb/s IPv4 packet forwarding
  - 2.5 Gb/s traffic manager
  - 3G basestation

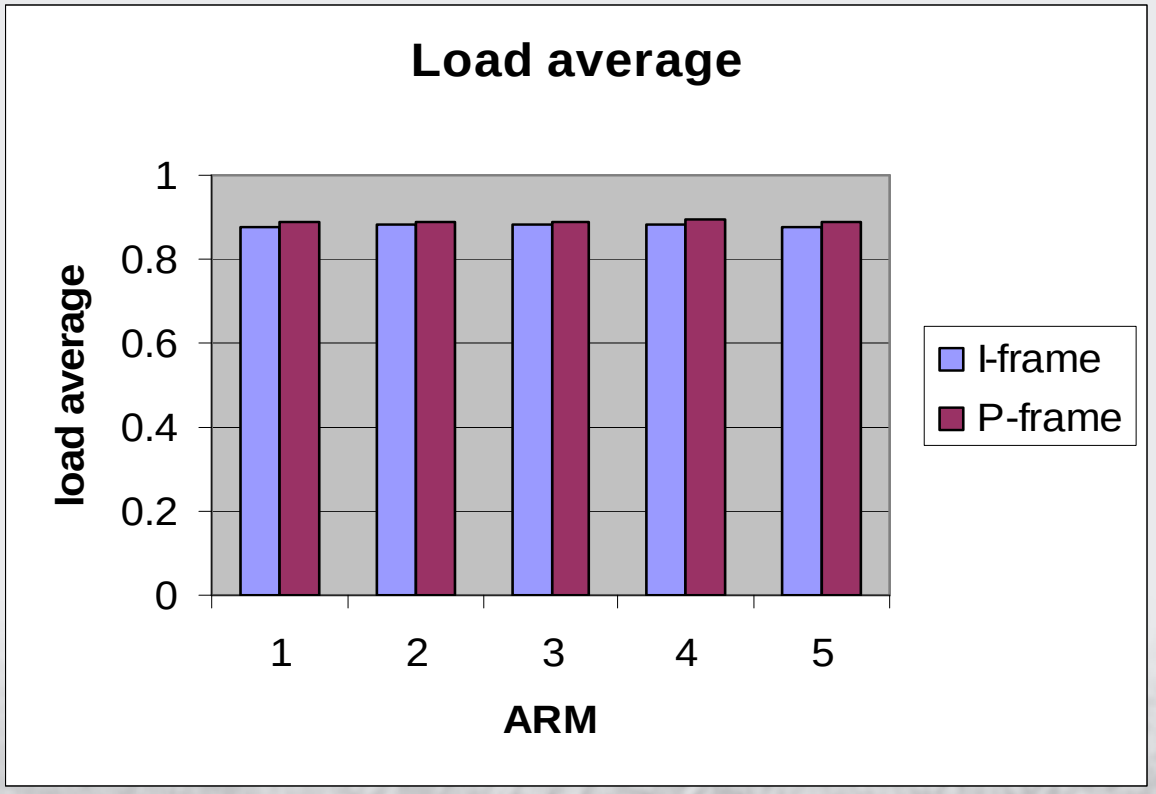
MPEG4 Codec Exploration

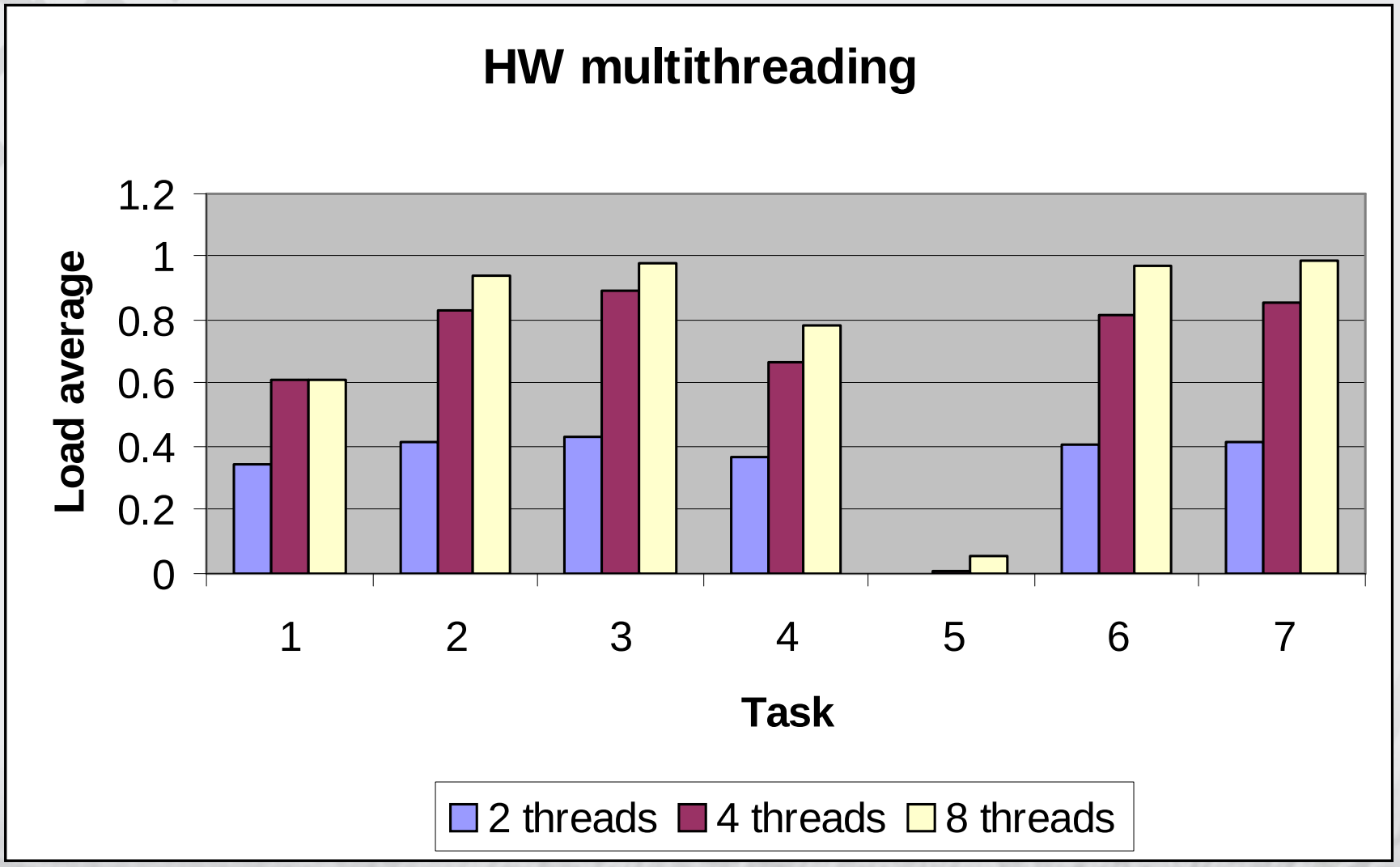
- 30 frame/sec, VGA resolution (4.1 GIPS required)
- High-level model using SMP and Message Passing



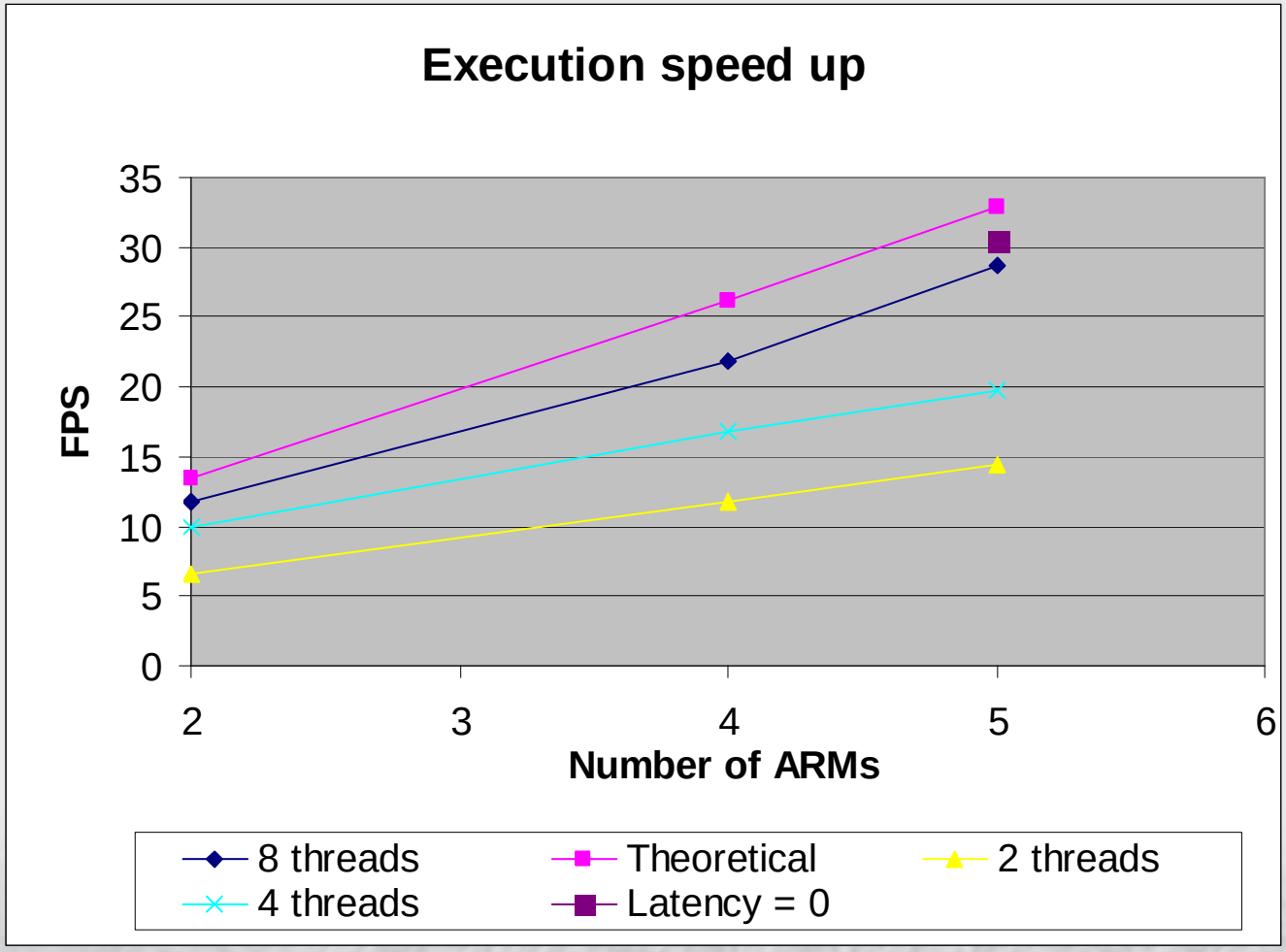
Load balancing

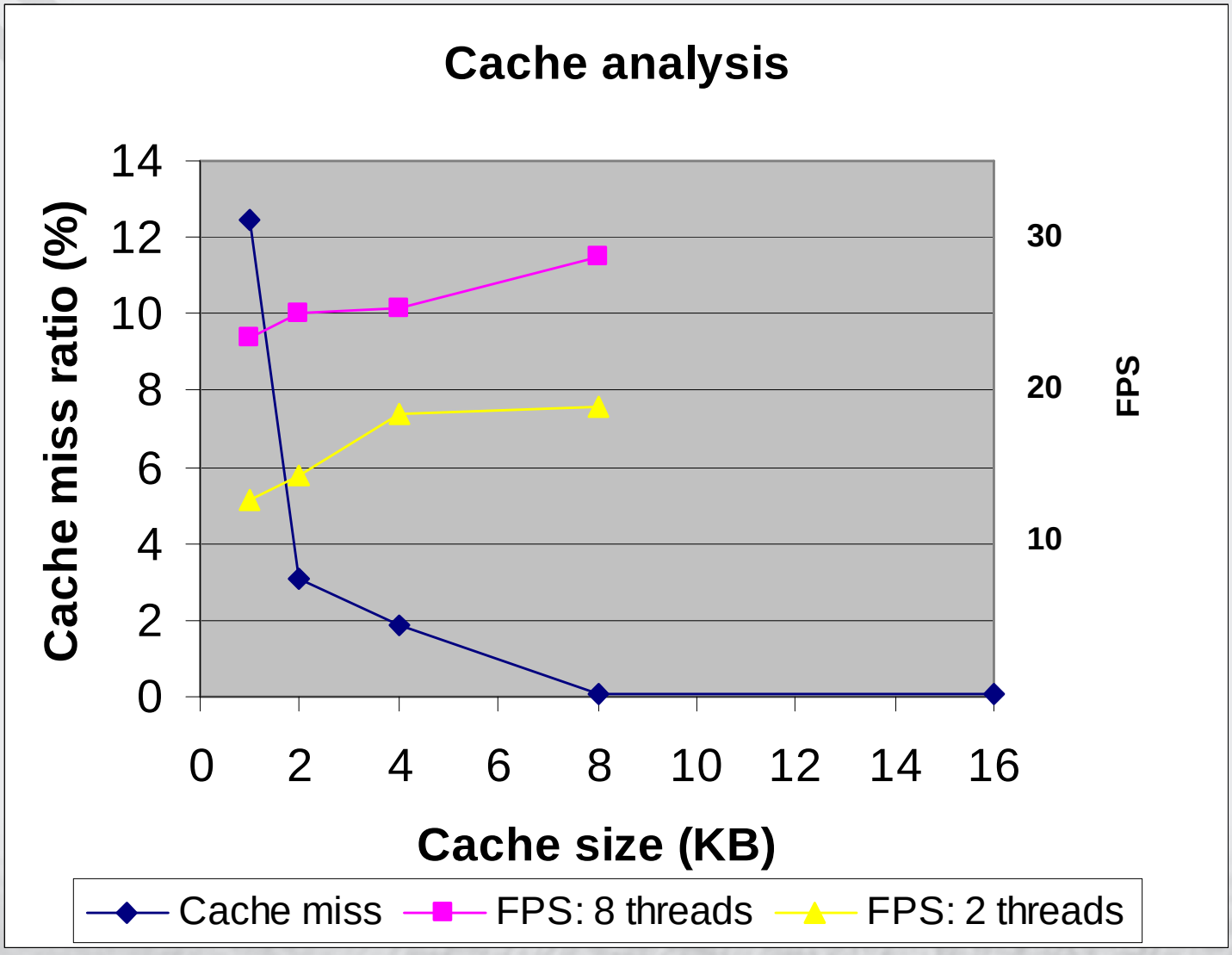
- The total load average is about 88%
- The load is well balanced over the 5 ARMs thanks to concurrency engine



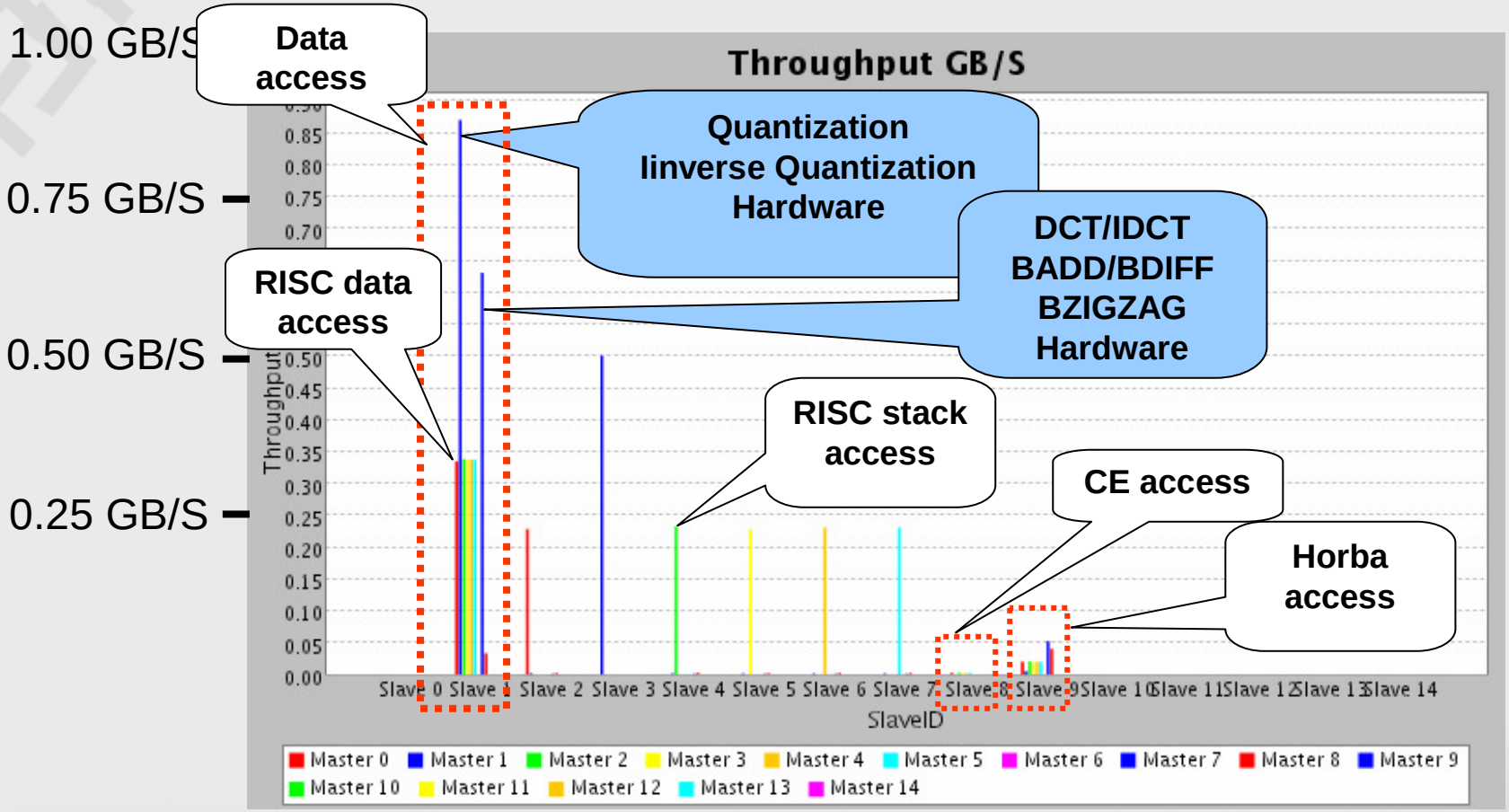

HW multithreading
Load average
1.2
1
0.8
0.6
0.4
0.2
0
1
2
3
4
5
6
7
Task
2 threads
4 threads
8 threads

Execution speed up

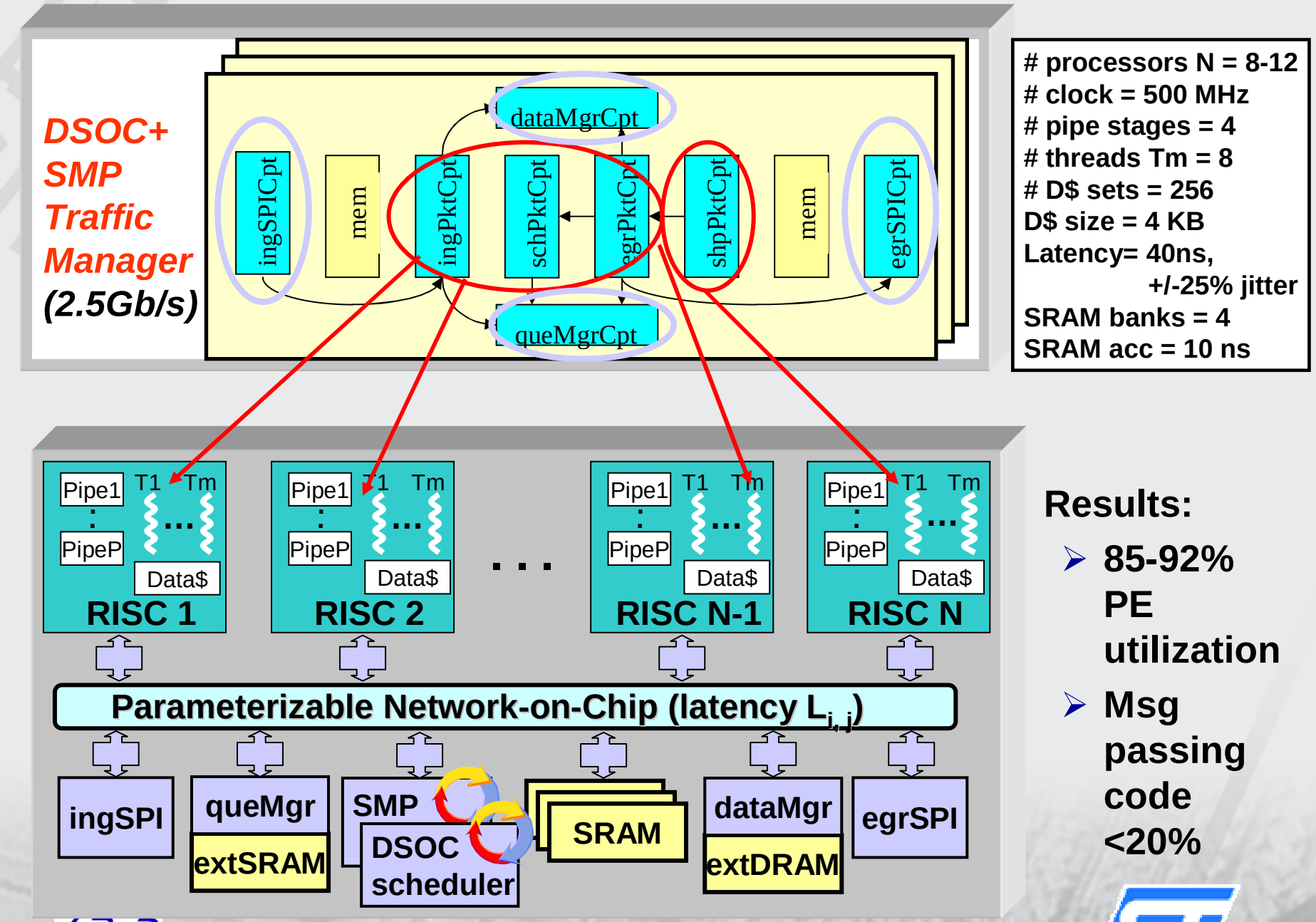



Cache analysis
Cache miss ratio (%)
14
12
10
8
6
4
2
0
30
20
10
FPS
0
2
4
6
8
10
12
14
16
Cache size (KB)
Cache miss
FPS: 8 threads
FPS: 2 threads

Local Noc Data Bandwidth (p-frame)



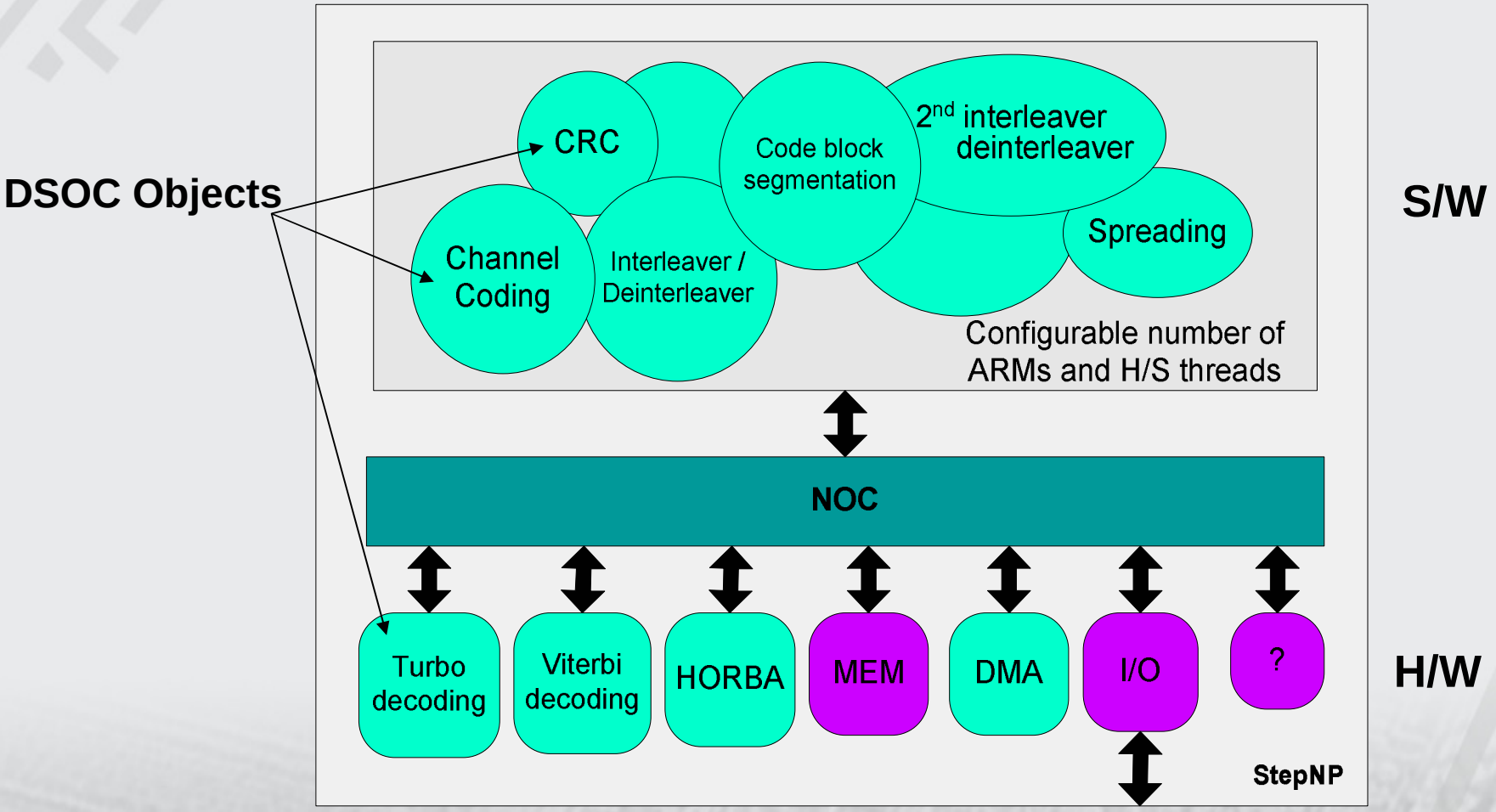
- Use of H/W load balancing engines (CE and HORBA)
  - **Only 3.8% data bandwidth overhead**



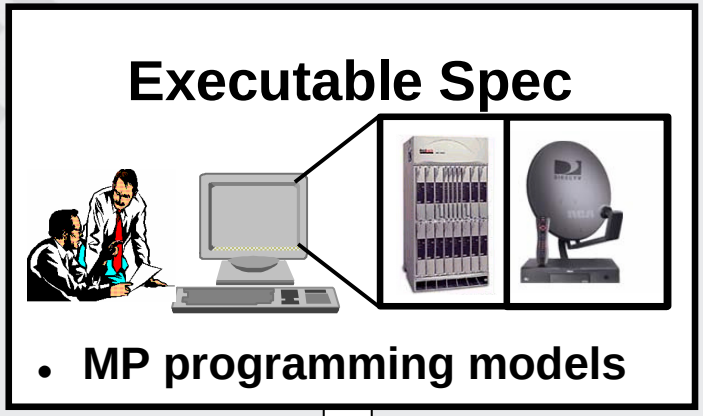
Results:

- 85-92% PE utilization
- Msg passing code <20%

3G Basestation Platform Exploration



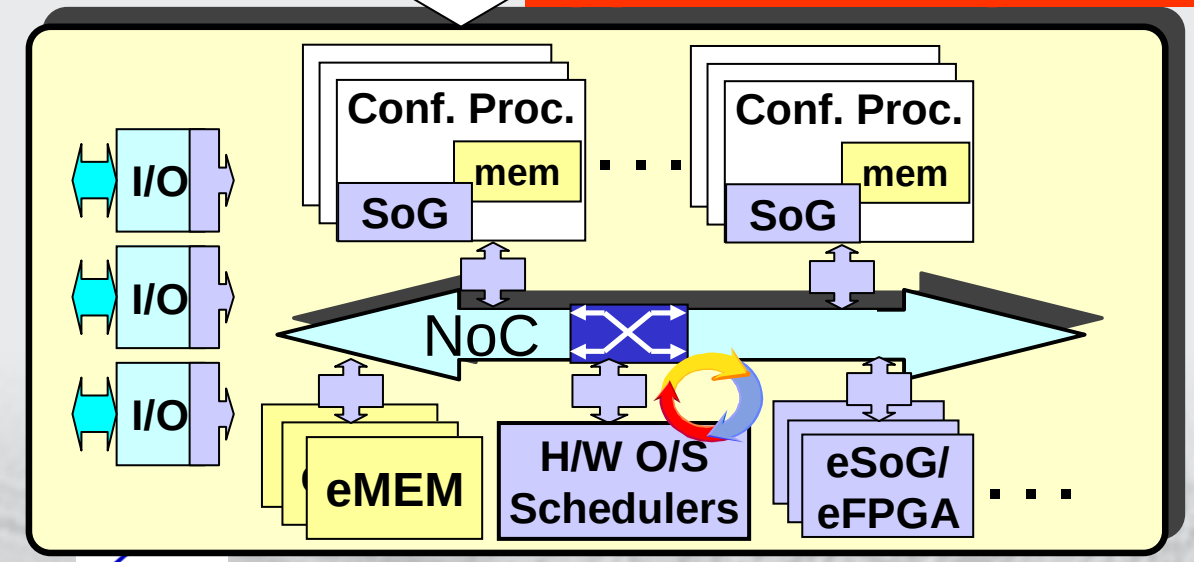
MultiFlex MP-SoC Tools: Summary



Value-added:

- Platform independent eS/W
- Platform scalability
- High PE utilization (85-97%)
- Ease of programming

Application to platform mapping



- Multi-media
- Networking
- 3G basestation