The Configurable Processor Company

IP Reuse and Integration in MPSoC: Highly configurable processors

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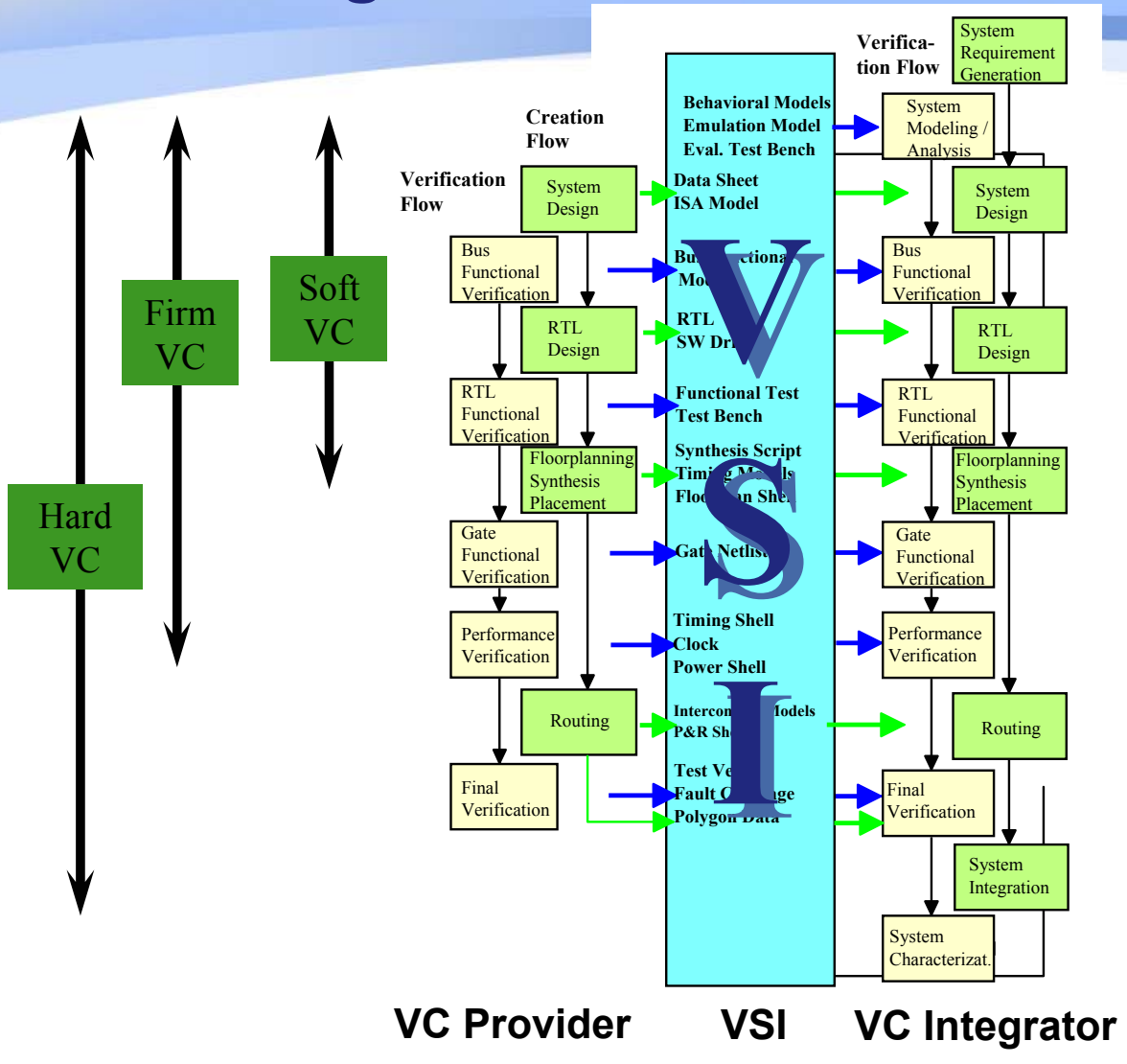
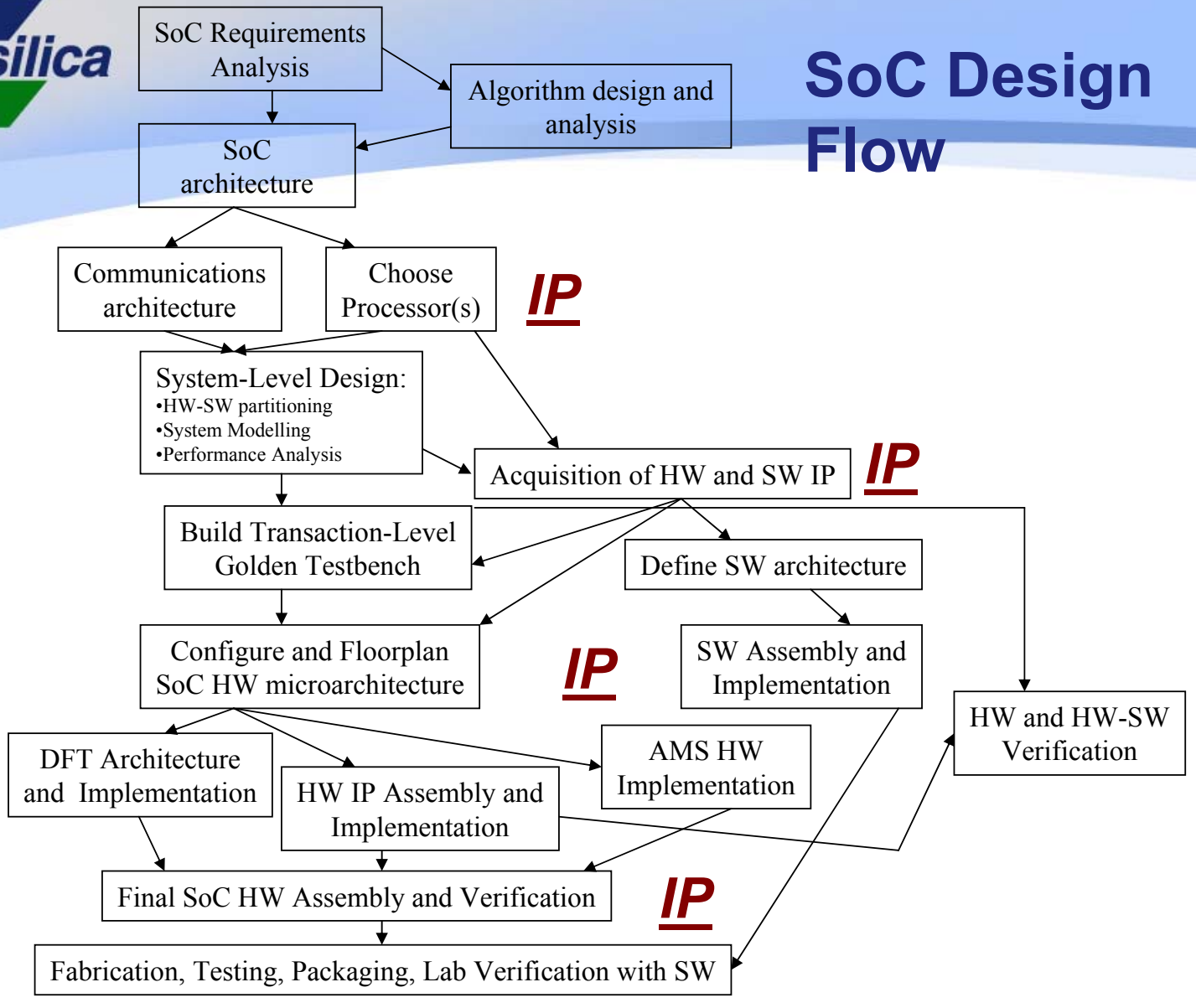
Outline

- “Static IP” Creation and Integration
- “Highly Configurable IP” Creation and Integration
- Emerging Standards

VSI Design Methodology: IP Creation and Integration



SoC Design Flow



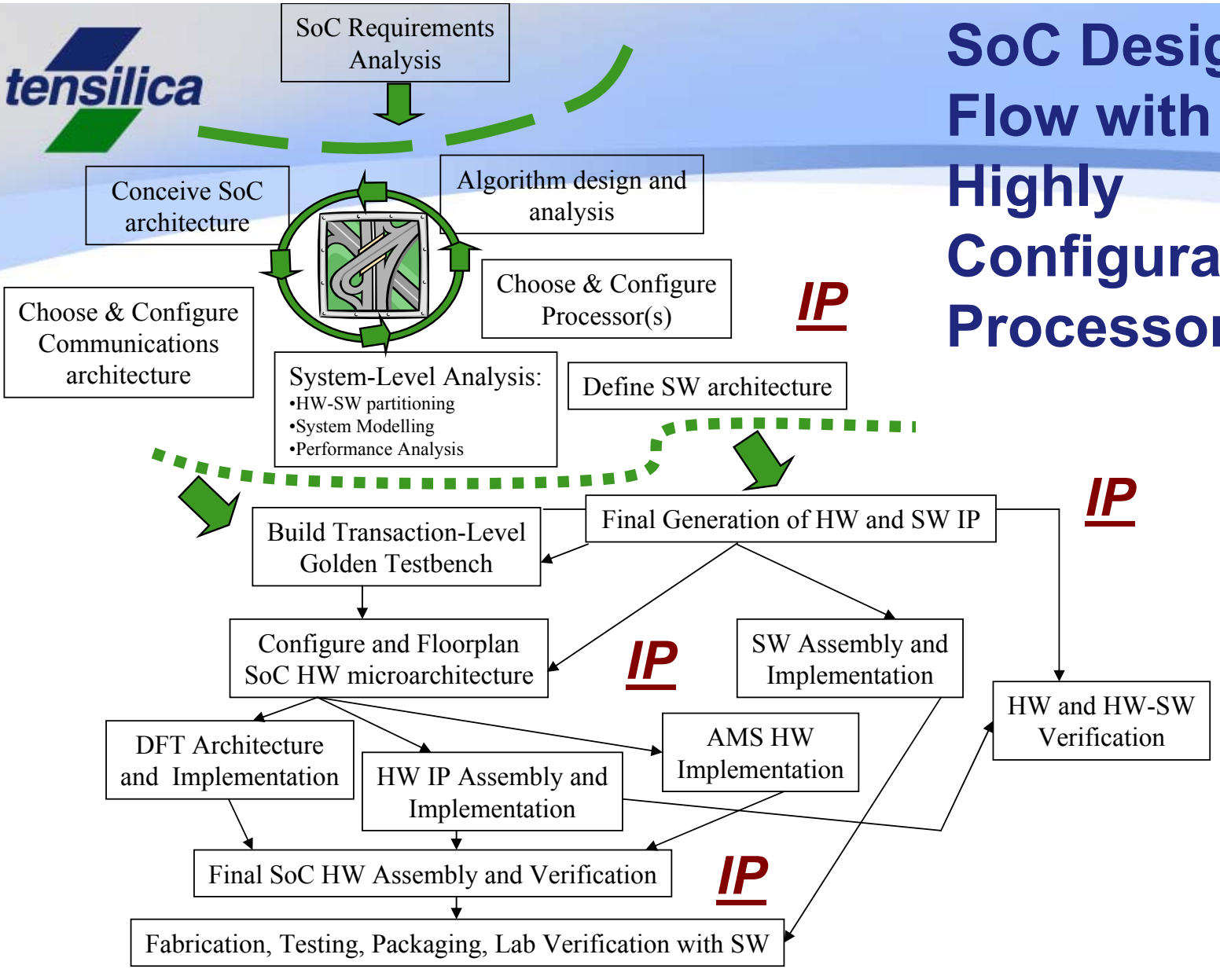
Evaluating the Quality of "Static IP": e.g. The VSIA Quality IP Assessment Metric

VirtualComponentName VCVendorCompany Copyright © 2003 VSIA	Scoring Summaries	
	IP Ease of Reuse	0%
	Design & Verification Quality	0%
	IP Maturity	0%
	Vendor Assessment	0%
Summary Report	Total	0%
	Design Quality	0%
Beta Release	Verification Quality	0%
Technical Support	Answers that are unacceptable	0
	Answers that are acceptable but add risk	0
	Answers that are acceptable	0
	Total	0
IPNAME	VirtualComponentName	
SupplierName	VCVendorCompany	
Select the type of block you are evaluating	mixed-signal IP	
Are you the IP developer or the end-user	Spreadsheet reviewer	
Are you interested in a traffic light report	Yes	
	Score	**%**
IP Maturity Assessment	0	0%
Vendor Assessment	0	0%
IP Ease of Reuse (IP Integrator's View)	0	0%
Documentation Quality	0	0%
Digital Soft IP: Documentation Quality	0	0%
Digital Verification IP: Documentation Quality	0	0%
Embedded Software: Documentation Quality	0	0%
Analog IP: Documentation Quality	0	0%
Ease of Integration	0	0%
Digital Soft IP: Reusability	0	0%
Digital Verification IP: Reusability	0	0%
Embedded Software: Reusability	0	0%
Analog IP: Reusability	0	0%
Design & Verification Quality (IP Developers' View):	0	0%
Design Quality	0	0%
Digital Soft IP: Design Quality	0	0%
Digital Verification IP: Design Quality	0	0%
Embedded Software: Design Quality	0	0%
Analog IP: Design Quality	0	0%
Verification Quality	0	0%
Digital Soft IP: Verification Quality	0	0%
Digital Verification IP: Verification Quality	0	0%
Embedded Software: Verification Quality	0	0%
Analog IP: Verification Quality	0	0%

IP Qualification

- **Some industry standards – MORE, OpenMORE, VSIA Quality DWG (Quality IP Metric)**
- **Self-applied: publicity**
- **Lack of 3rd party certification**
- **Many organisations certify incoming IP quality themselves**
- **3rd party providers rely more on reputation than facts – their customers must provide the facts:**
  - "Measuring IP quality costs time and effort. Many of the large system and semiconductor companies have spent the last seven years creating in-house IP quality procedures, and a number of them claim it costs as much as 3 man-months to verify the quality of one single piece of IP."
    - Larry Cooke, "Why we don't have IP quality yet", EEDesign (online), July 24, 2003
- **Relevance to Highly Configurable IP must be considered**
  - Qualify the Generated IP or Qualify the Generation Process?
  - If you use a lot of generated IP, you should think about Process not Results
- **Conclusions:**
  - There is no current substitute for inspecting, QA'ing and certifying incoming 3rd party IP yourself
  - The reputation of the supplier is a key component of IP Quality
  - For highly configurable IP, the generation process controls the output quality

SoC Design Flow with Highly Configurable Processors



Configurable vs. Relatively static Processor IP

- **Configurable Processor IP is the result of a configuration process**
  - Not a static deliverable
  - Not a lightly configured design – ie. Choosing one of a few pre-defined configurations, or choosing parameter values from ranges for a few simple option
- **This process is driven by specifying a configuration in some kind of GUI**
  - Many degrees of variability
  - Many interlocking options
  - Need to capture valid combinations and ranges of options in complex rules
  - Users require the support of some kind of estimators to give them a reasonably accurate feeling for the key characteristics of the output of the process
    - E.g. power, area (cost), performance
- **Ideally, the process should run in a few hours at most to provide rapid feedback and iteration or design space exploration**
  - Output deliverables must then allow complete implementation and verification in standard EDA flows

Examples of possible coarse-grain configuration options for processors

Control & State

- Register size
- Interrupts / priority
- Timers
- Debug breakpoints
- Trace port
- Boolean registers
- Processor ID register
- Scan & clocking options

Execution Units

- Floating point
- DSP Options
  - 16 bit MAC
  - Special DSP hardware (eg. SIMD)
- Multiplier, 16 or 32 bit

Memory and Interface

- Cache - Instruction & Data
  - Size, e.g. to 32KB, 1 to 4 way
  - Writeback or Write Thru (Data)
  - Line Locking (Data & Instruction)
- Local RAM/ROM
  - Instruction & Data
- Memory protection / MMU
- Local Memory Interface ports with flow control
- Processor bus Interfaces
  - Include / Exclude (optional)
  - 32, 64 or 128 bit interface
  - Write Buffer depth
  - Incoming Request (DMA) Support

Support of generation process with estimators

- **With a huge variety of coarse-grained configuration options, users need basic feedback on the likely outcome of the generation process**
  - In terms of power, performance, area (cost)
- **Estimators must be based on parameter sweeps over technology choices.**
  - With near-infinite numbers of possible configurations, must sweep over a suitable subset of possibilities
  - Corner cases
  - Ends of parameter ranges
  - Build estimators and predictors, and understand montonicity and sensitivity
  - As an example, Tensilica uses a database compiled from >200 post-layout (full place and route) designs for Xtensa 1050 core. This uses a compilation of 3rd party libraries representing several commercial COT foundry processes.

Additional configuration possibilities for processors

- **Instruction extensions – to adapt configurable processors much more closely to applications**
  - "fine-grain" configuration, complementing "coarse-grain" options
- **A variety of choices**
  - Some offer co-processor creation – partial implementation of intensive data processing portions of algorithms (e.g. loop nests)
    - May allow creation of several coprocessors
    - Loosely coupled to main processor instruction processing
      - Often processor core will stall while coprocessors operate
  - As a contrasting example, the Tensilica T1050 and LX cores allow instruction extensions to be compiled into dedicated hardware deeply embedded in the main processor datapath
    - These are then directly supported in the generated software toolkit
    - Instruction extensions are described in a special format called TIE which supports both structural and semantic description mechanisms for a particular instruction, which may be multi-cycle

Required output deliverables from processor configuration

- **SW development environment**
  - Compilers – C/C++, and SW libraries
  - Operating System support
  - Links to Integrated Development environments (IDEs) including debugging, build processes, configuration management, profiling, etc.
  - As an example, Tensilica offers an IDE environment based on Eclipse called xPlorer (users also are able to use other IDEs); optimised compiler generation (xcc), and links to standard OS's (e.g. WindRiver)
- **System level modelling and debugging**
  - Instruction Set Simulator (ISS)
  - Multi-core system modelling environment (usually C/C++-based, or SystemC)
  - HW-SW Co-simulation model support
  - Emulation or rapid prototyping support
  - For example, the Tensilica generation and build process produces:
    - ISS in standalone mode, in IDE (xPlorer), and in multi-core C++ system modelling environment (XTMP) which also can be interfaced with SystemC
    - Support for Mentor Seamless HW-SW cosimulation
    - Support for FPGA-based emulation boards

Additional required deliverables – implementation and verification flows

- **Implementation and verification of configured IP requires support for highly automated flows**
  - Synthesis, placement, routing, verification
  - Need to rely on standard leading EDA tools
  - Must be very responsive to customer pull on flows without spending large support efforts on small minority flows
  - Similar issue on support for design languages – support most commonly used; cannot leap on new languages (e.g. SystemVerilog) until sufficient customer pull
  - Quality of output is paramount, and thus support for advanced verification methods important
- **As an example, Tensilica supports Verilog and VDHL outputs, Synopsys synthesis, Synopsys and Cadence P&R and timing, Synopsys, Cadence and Mentor simulators.**
  - In addition, support for extraction, power analysis, test, co-simulation, equivalence checking, assertion based verification, and testbench languages using leading EDA suppliers in each category.

Evaluating the Quality of Highly Configurable IP

Programmers' Reference Manual	
Does this component contain a programmable instruction set ?	y/n
If this IP block is instruction programmable, then a software reference manual is required. Is a software reference manual available?	y/n
Memory organization	y/n
Instruction Registers	y/n
Operand Size and Addressing	y/n
Data types	y/n
Instruction Set	y/n
Procedure Calls, Interrupts, Exceptions	y/n
Input-Output Processing	y/n
Does this component contain a programmable register set ?	y/n
Is there a register map section present in the hardware reference manual or a separate document available that describes how to program the registers?	y/n

(Extracts From VSIA QIP Assessment Metric)

Ease of Integration (IP Integrator View)	
Configurability and Parameterization	
Is the IP configurable?	y/n
Is the IP designed to support instance by instance configurability?	y/n
Is the configuration accomplished thru the establishment of parametric calling routines rather than modifying hard coded constants?	y/n
Are configuration examples provided?	y/n
Are all configuration parameters clearly defined and documented?	y/n

- **Current assessments are geared towards static IP, not highly configurable processors**
- **Current methods evaluate outputs, not process for configuration, generation and use**
- **Users need to adapt these methods in assessing suppliers of highly configurable IP**

The Business of IP Integration: Existing and Emerging Standards, Companies and Organisations

SYSTEMC™

Welcome to the SystemC Community

VSI Alliance™

SystemC OCP Models Now Available

OCP International Partnership

VIRTUAL COMPONENT EXCHANGE

VCX™

-SPIRIT-

Design And Reuse

The Catalyst of Collaborative SoC Design through SIP Exchange

FABLESS SEMICONDUCTOR ASSOCIATION

accellera

What are some of these organisations doing?

- **VSIA – standards for IP creation, interchange and use**
  - VSIA IP Quality metric already discussed
  - VSIA restructuring (May-June 2004) has kept Quality focus
- **VCX – was going to be a "SOC Exchange" (for IP)**
  - Becoming a software company
- **FSA – collaborating with VSIA on IP quality**
  - Intellectual Property Committee
- **Open SystemC International (OSCI)**
  - Transaction Level Modelling Standards
- **Open Core Protocol International Partnership (OCP-IP)**
  - A particular bus/interface standard based on SONICS
- **SPIRIT**
  - Standards for defining IP and Platform "Meta-Data"

The SPIRIT Consortium

The SPIRIT Consortium

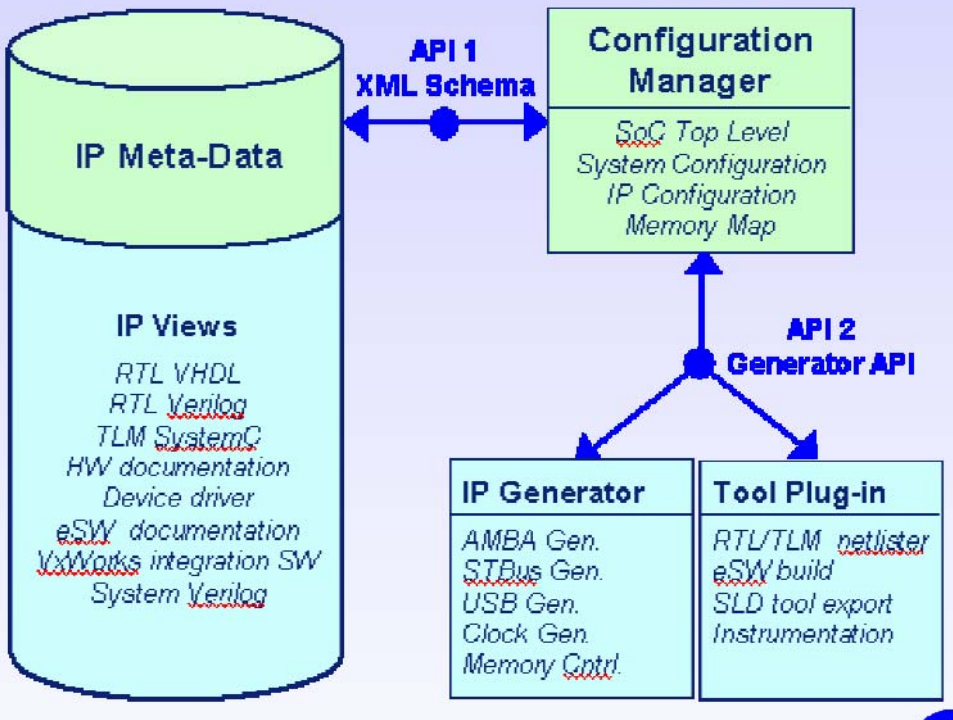
- **SPIRIT**
  - **S**tructure for **P**ackaging, **I**ntegrating and **R**e-using **I**P within **T**ool-flows
  - A consortium of leading companies in the EDA, IP, system and semiconductor industries
- **Aim**
  - To develop industry standards
    - Ease integration of semiconductor IP into Systems
    - Enable the interoperability of tools for IP integration

SPIRIT

ARM cadence Mentor Graphics PHILIPS synopsys

Source: SPIRIT Press Presentation, SAME, October 2003

SPIRIT concept



ARM cadence Mentor Graphics PHILIPS SYNOPSYS

Source: SPIRIT Press Presentation, SAME, October 2003

Some Observations about Standards

- **VSIA**
  - I think its day is done – accomplished what it could
  - FSA IP committee may hold more industry credibility
  - Restructuring May-June 2004 may or may not succeed – but reduced VSIA scope
- **OSCI**
  - Valuable but seems slow and politics is mounting
  - TLM work has strong potential for system-level IP models – but its late
    - (at DAC 2004, implication of 2.1 release this summer and TLM by Fall 2004)
- **SPIRIT**
  - Meta-data interchange standard in XML is potentially useful
  - Web site talks about first standard out end of 2003…..the clock is ticking. At DAC 2004, first phase (RTL) promised end October 2004.
- **In all these cases – the absence of agreed industry standards perpetuates ad-hoc solutions – at a cost**
  - Tensilica had to create its own C/C++-based Transaction Level Modelling System simulation capability
  - We also have created something which has the flavour of part of the SPIRIT concept for internal use

Conclusion

- **IP reuse remains one of the big design challenges**
- **Quality is issue number one**
  - But quality has to be assessed by integrators
  - Reputation is possibly the best guide today
- **Methods for static IP need considerable adaptation to cope with highly configurable IP**
- **Standards have a role**
  - BUT standards organisations seem to be bogging down
  - Overly ambitious
  - The politics and economics of EDA seem to trump the interests of the IP creators and users
  - Unclear that this will change
  - If not, ad-hoc proprietary solutions must continue to be invented