MPSoC '08

8th International Forum on
Application-Specific Multi-Processor SoC
23 - 27 June 2008
Château St. Gerlach, Valkenburg a.d. Geul, Netherlands

FOCUS

MPSoC is a pluridisciplinary forum bringing together key R&D actors from the different fields required to design heterogeneous Multi-Processor SoC (MPSoC). The full week format and the quality of both attendees and speakers make of MPSoC a unique occasion for executives and senior managers to explore new ideas and refine strategic thinking.

CONTENTS

The program brings together key actors from IP, fabless, semiconductor, system houses and design industry to build a vision of the next steps in integrated system design. More than 50 world class R&D speakers will discuss **fundamental and strategic issues to master multi-processor SoC design**. The program includes serveral keynotes and 4 days to present strategic directions and state-of-the-art research. The goal is to discuss challenges and opportunities for future SoC applications and technologies.

WHY ATTEND

MPSoC features an excellent technical program, with lots of interactions, in a great setting. The combination of people, content and setting allows for **more relationships and ideas being formed in a few days than in a month of doing anything else**. The confluence of academic and industrial perspectives, hardware and software perspectives, IP and system challenges, technology vision and business strategies makes MPSoC unlike other conferences, seminars and exhibitions.

INFORMATION

REGISTRATION, ACCOMMODATION, VENUE, and further INFORMATION:

www.mpsoc-forum.org

Sponsored by
European Design and Automation Association, and IEEE Council on Electronic Design Automation

General Co-Chairs:
Heinrich Meyr, Institute for Integrated Signal Processing Systems (ISS), RWTH Aachen University, Germany
Rainer Leupers, Chair for Software for Systems on Silicon (SSS), RWTH Aachen University, Germany

Local Organisation Chair:
Gerd Ascheid / Ute Müller, Institute for Integrated Signal Processing Systems (ISS), RWTH Aachen University, Germany

Finance Chair:
Heinrich Meyr / Tamara Durant, Institute for Integrated Signal Processing Systems (ISS), RWTH Aachen University, Germany

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Hannu Tenhunen, Swedish Royal Academy, Sweden
Wayne Wolf, Georgia Institute of Technology, USA
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Norbert Wehn, University of Kaiserslautern, Germany
Drew Wingard, Sonics, USA
Wayne Wolf, Georgia Institute of Technology, USA
Hiroto Yasuura, Kyushu University, Japan
Yervant Zorian, Virage Logic, USA

MPSoC '08

ADVANCE PROGRAM

18.00 Registration
19.00 Welcome reception

Monday June 23

8.00 Registration

SESSION 1: KEYNOTE

8.55 Heinrich Meyr, Chairman MPSoC'08
Opening remarks

9.00 Liang-Gee Chen, National Taiwan University, Taiwan
Reconfigurable and Scalable Stream Processor for Multimedia Application

10.00 Break

SESSION 2: MINI-KEYNOTES

10.30 Paolo Ienne, EPFL, Switzerland
Analytical Models of Communication

10.45 Youn-Long Lin, National Tsing Hua University, Taiwan
Memory Access Analysis and Optimization for Ultra High Definition Video Decoding

11.00 Vijaykrishnan Narayanan, Pennsylvania State University, USA
Network on Chips for 3D Chips

11.15 Marcello Coppola, STMicroelectronics, France
Spidergon: STNoC: The Communication Infrastructure for Multiprocessor Architectures

11.30 Pier Stanislao Paolucci, ATMEL & INFN, Italy
Four Levels of Parallelism to be Managed in the DIOPSIS based SHAPES Multi-Tiled Architecture

11.45 Panel discussion with the lecturers
12.15 Lunch

SESSION 3: IN-DEPTH TECHNICAL PRESENTATIONS

13.45 Jörg Henkel, University of Karlsruhe, Germany
Adaptive Embedded Processing with RISPP

14.15 Takashi Miyamori, Toshiba, Japan
Venezia: a Scalable Multicore Subsystem for Multimedia Applications

14.45 Jason Parker, Symbian Ltd., UK
The opportunity and challenges of SMP in the mobile phone

15.15 Break

15.45 René van den Berg, NXP, Netherlands
Predictable and Composable Multiprocessor Systems for Car-Entertainment: Breaking Cyclic Dependencies. Part 1: business view

16.15 Marco Bekooij, NXP, Netherlands
Predictable and Composable Multiprocessor Systems for Car-Entertainment: Breaking Cyclic Dependencies. Part 2: research view

16.45 Panel discussion with the lecturers
19.00 Dinner

Tuesday June 24

SESSION 4: KEYNOTE

8.30 Tim Kogel, CoWare, Germany
Using the new TLM-2.0 standard for the Creation of Virtual Platforms for ESL Design

9.30 Break

SESSION 5: MINI-KEYNOTES

9.45 Soonhoi Ha, Seoul National University, Korea
Embedded Software Development for MPSoC: Preliminary HOPES Experience

10.00 Masaharu Imai, Osaka University, Japan
Architecture Level Power Reduction Method for Configurable Processor Generation

10.15 Hironori Kasahara, Waseda University, Japan
Compiler and API for Low Power High Performance Multicores

10.30 Joachim Kunkel, Synopsys, USA
MPSoC IP Integration and Interoperability Challenges

10.45 Jan Madsen, Technical University of Denmark
Adaptive Embedded Systems – Challenges of Run-Time Resource Management

11.00 Break

SESSION 6: IN-DEPTH TECHNICAL PRESENTATIONS

11.15 Gerd Ascheid, RWTH Aachen University, Germany
MPSoC Design Space Exploration Framework

11.45 Katalin Popovici, Mathworks, France
Software Design and Integration for Embedded Applications by Successive Refinement

12.15 Rudy Lauwereins, IMEC, Belgium
Will 3D Stacking of ICs Enable to Continue Moore's Momentum in the 21st Century?

12.45 Panel discussion with the lecturers
13.15 Lunch
14.15 Social Event (Aachen, Germany)
19.15 Dinner, Aachen, Germany

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Wednesday June 25

SESSION 7: KEYNOTE

8.30 **Luca Benini, University of Bologna, Italy**
3D-MPSoCs: Architectural and Design Technology Outlook

SESSION 8: MINI-KEYNOTES

9.30 **Omar Hammami, ENSTA, France**
Heterogeneous Embedded Systems Very Large Scale Design Space Exploration

9.45 **Jari Nurmi, Tampere University of Technology, Finland**
Silicon Café: a Heterogeneous Multi-Processor Platform based on Coffee (RISC Core)

10.00 **Atsuhiro Suga, Fujitsu Laboratories, Japan**
A-RPC based Heterogeneous Multicore Platform Suitable for an Embedded System

10.15 **Break**

10.45 **Thierry Collette, CEA LIST, France**
Key Technologies for Hundred-Core Architectures

11.00 **Olivier Franza, Intel, USA**
Power Mitigation Techniques in complex MPSoCs

11.15 **John Goodacre, ARM, UK**
The Effect and Technique of System Coherence in ARM Multicore Technology

11.30 **Steven P. Levitan, University of Pittsburgh, USA**
Zooming out and Scaling up: from 1 to 1000 Cores

11.45 **Kazutoshi Wakabayashi, NEC, Japan**
Practical Usage of C-based Design

12.00 **Pieter van der Wolf, NXP, Netherlands**
Performance Contracts for Modular MPSoC Integration

12.15 **Panel discussion with the lecturers**

12.45 **Lunch**

SESSION 9: IN-DEPTH TECHNICAL PRESENTATIONS

14.15 **David Atienza, LSI, EPFL, Switzerland**
New Exploration Frameworks for Temperature-Aware Design of MPSoCs

14.45 **Stefan Heinen, RWTH Aachen University, Germany**
Challenges for SoC Integration of Multistandard-RF-Circuits

15.15 **Christian Piguet, CSEM, Switzerland**
Design Methodologies for Heterogeneous Systems and Case Studies of MPSoC Chips

15.45 **Break**

SESSION 10: MINI-KEYNOTES

16.15 **Dominique Ragot, THALES, France**
MPSoC Architecture Low Power Optimisation under Linux

16.30 **Lothar Thiele, ETH Zürich, Switzerland**
Closing the Loop: Exploration and Estimation

16.45 **Steve Leibson, Tensilica, USA**
Green Computing: What does it mean for embedded silicon systems?

17.00 **Yankin Tanurhan, ACTEL, USA**
Low Power Solutions in FPGA based Program-mable Heterogeneous Multi-Processor Systems

17.15 **Panel discussion with the lecturers**

19.00 **Dinner**

Thursday June 26

SESSION 11: KEYNOTE

8.30 **Wanda Gass, Texas Instruments, USA**
Gaining Focus: Developing a "Tops-Down" Approach to Multicore Processor Architectures

9.30 **Break**

SESSION 12: MINI-KEYNOTES

10.00 **Soo-Ik Chae, Seoul National University, Korea**
A RISC Cluster for a H.264 D1 Software Decoder

10.15 **Ahmed Jerraya, CEA-LETI, MINATEC, France**
System Compilation for MPSoC based on NoC

10.30 **Ulrich Ramacher, Infineon, Germany**
R&D for X-Gold SDRxx Baseband Processors

10.45 **Norbert Wehn, University of Kaiserslautern, Germany**
An Outer Modem ASIP for Software Defined Radio

11.00 **Rolf Ernst, Technical University, Braunschweig, Germany**
Load Level Modeling

11.15 **Panel discussion with the lecturers**

12.00 **Lunch**

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SESSION 13: IN-DEPTH TECHNICAL PRESENTATIONS

13.30 Kevin Smart, Synopsys, UK
Virtually Solving Debug Challenges of the MPSoC Era

14.00 Tsuyoshi Isshiki, Tokyo Institute of Technology, Japan
MAPS-TCT: MPSoC Application Parallelization and Architecture Exploration Framework

14.30 Achim Nohl, CoWare, Germany
Debugging and Test Techniques for Parallel Software using Virtual Platforms

15.00 Break

SESSION 14: MINI-KEYNOTES

15.30 Toshihiro Hattori, Renesas, Japan
Multi-Domain System Support Environment for Multi-Core System

15.45 Gabriela Nicolescu, Ecole Polytechnique de Montréal, Canada
Design Space Exploration for Applications Mapping on MPSoC Architectures

16.00 Frédéric Pétrot, TIMA - SLS, France
Timing Estimation for Native Software Execution in MPSoC

16.15 Eric Verhulst, OpenLicenseSociety, Belgium
Programming without Communication, the Key to Multi-Core and Distributed Programming

16.30 Panel discussion with the lecturers

19.00 Dinner

Friday June 27

SESSION 15: KEYNOTE

8.30 Gerhard Fettweis, TU Dresden, Germany
Challenges and Solutions for Building Future MPSoCs for Cellular Communications

9.30 Break

SESSION 16: IN-DEPTH TECHNICAL PRESENTATIONS

10.00 Michael Speth, Infineon, Germany
Design and Verification Challenges for G/3.5G/4G Wireless Baseband MPSoCs

10.30 Rakefet Kol, Zoran Microelectronics, Israel
Must Provide a Solution on a Chip – from concept to delivery

11.00 Jürgen Teich, University of Erlangen-Nuremberg, Germany
Reconfigurability Issues of Future Massively Parallel SoCs

11.30 An-Yeu Wu, Industrial Technology Research Institute, Taiwan
Overview of ITRI's Parallel Architecture Core (PAC) DSP Project

12.00 Panel discussion with the lecturers

12.30 Lunch

MPSOC'08 FORUM REGISTRATION FORM

For registration before May 11th, 2008, the fee amounts to 1200 EURO for regular attendees, 950 EURO for IEEE and EDAA members, and 750 EURO for students. It will cover the documentation, the lunch for five days, dinner for four days including the social dinner. 2 days registration before May 11th, 2008 amounts to 750 EURO.

Registration form and further information at: **www.mpsoc-forum.org/registration.html**

MPSOC'08 HOTEL RESERVATION

MPSoC'08 will be held on June 23-27, 2008 at Chateau St. Gerlach, Valkenburg, The Netherlands.
Chateau St. Gerlach
Joseph Corneli Allee 1
NL-6301 KK Valkenburg, The Netherlands
Phone: 0031-43-608 88 88
Fax: 0031-43-604 28 83
E-Mail: info@stgerlach.com (with reference: "RWTH Aachen GF15313")
It takes 30 minutes from Aachen (by car).

Room reservations should be made by May 31, 2008. Reservation condition after this date is subject to change.
Further reservation information and accommodation: http://www.mpsoc-forum.org/location.html
* Please note that there is no bank or ATM in the hotel, although you can make a payment with a credit card.