MPSOC Architectures for Computing for Imaging

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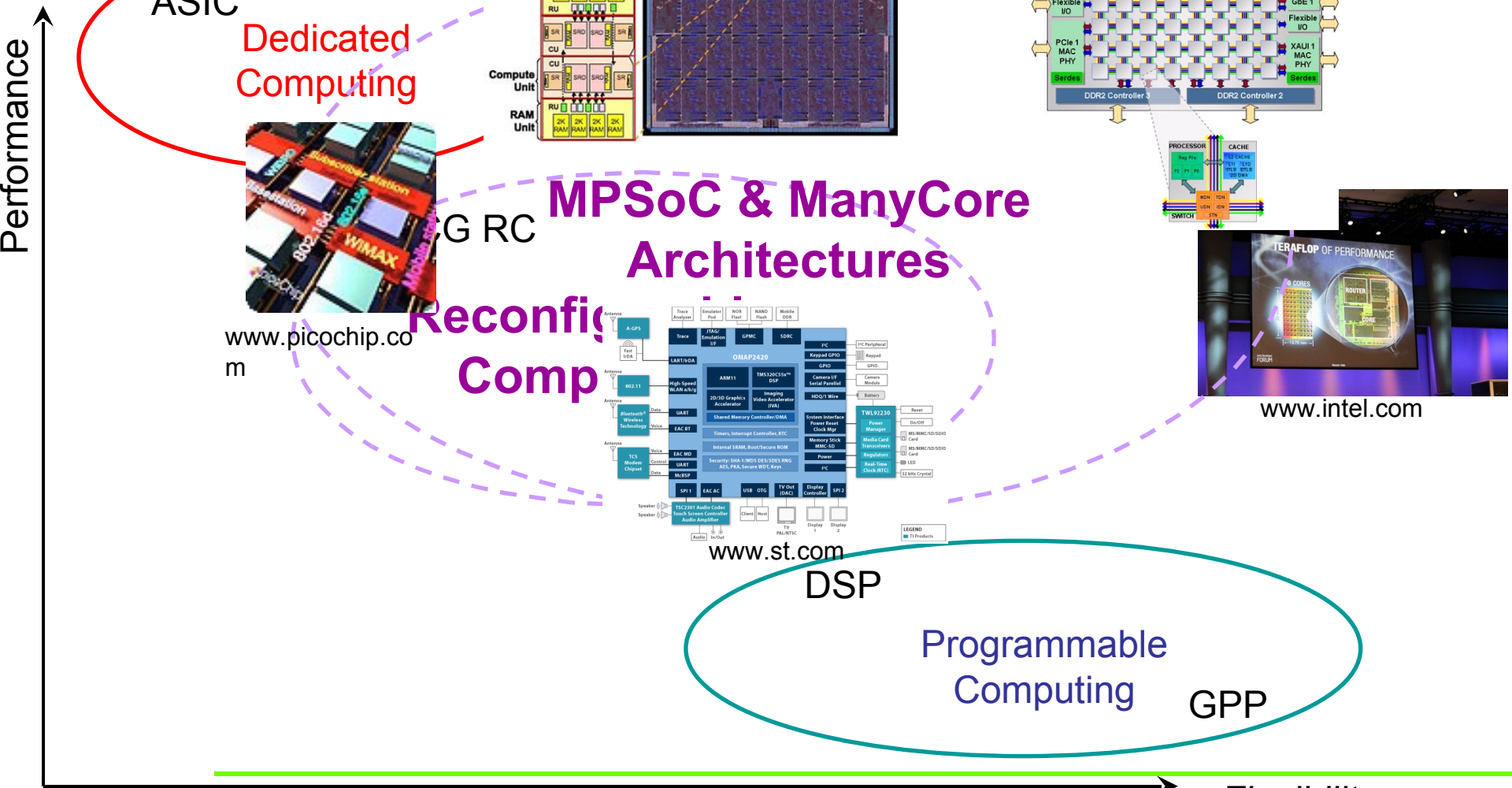
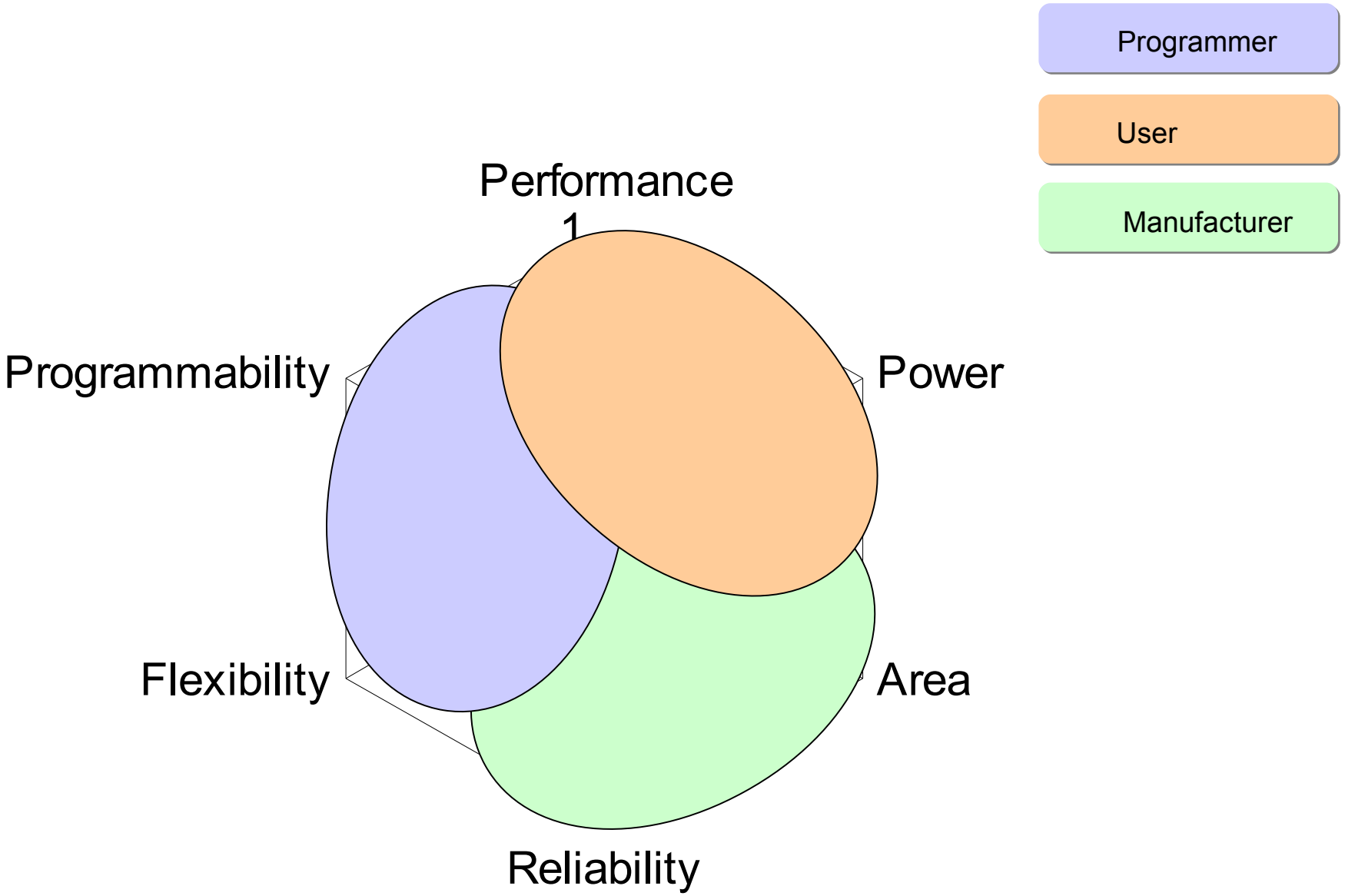
Embedded Computing: a New Area



Evaluation Criteria

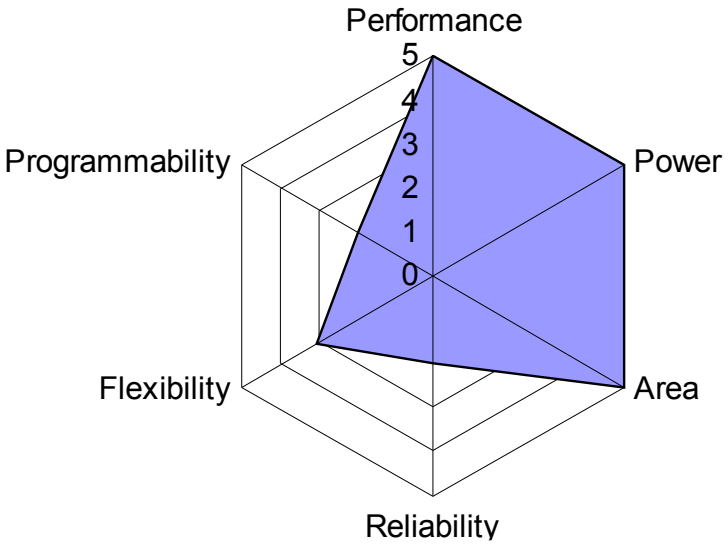
- **From the** User's **point of view:**
  - ✓ **Computing Performance**
  - ✓ **Power consumption**
  - ✓ **Application Reliability and Dependability**
- **From the** Programmer's **point of view:**
  - ✓ **Flexibility**
  - ✓ **Programmability**
- **From the** Manufacturer's **point of view:**
  - ✓ **Silicon Area**
  - ✓ **Hardware Reliability**

Design dilema of Embedded Computing Solutions

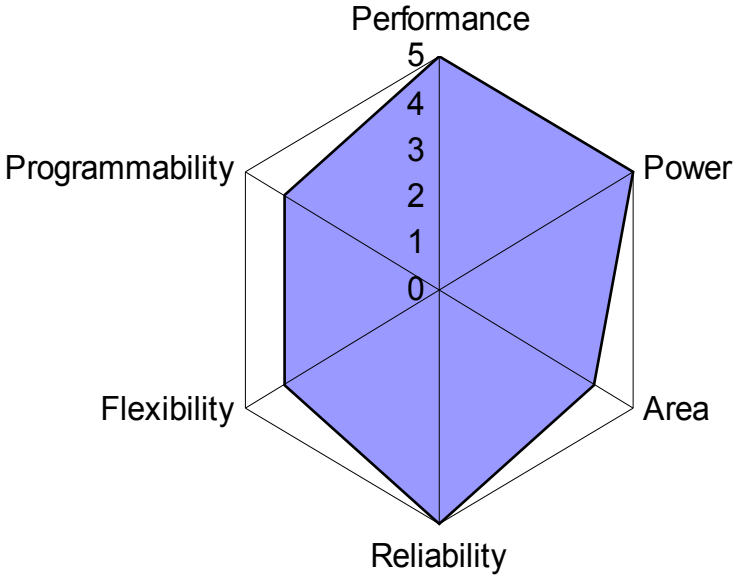


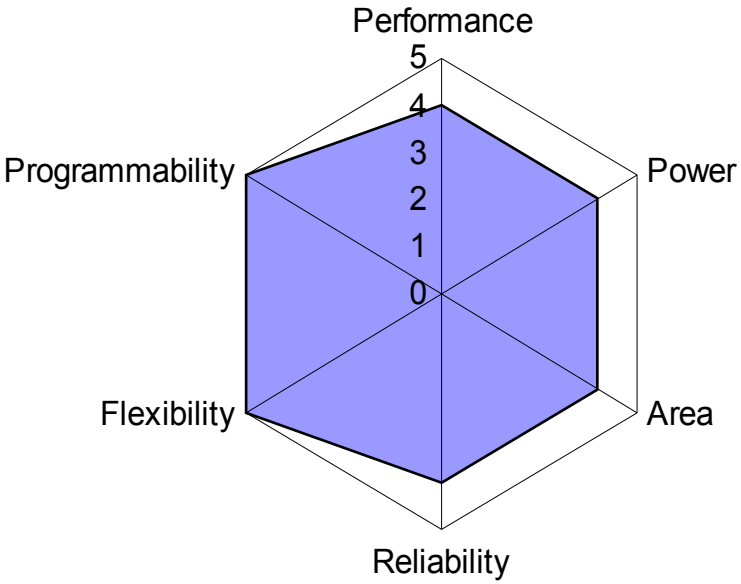
Different Architectures

Imaging



MPPA





Computing for Imaging at CEA LIST

With more than 20 years of experience in computer design for image processing

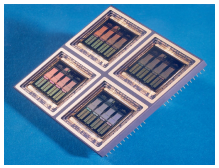
1990 — Sympati 1 µm

Line processor array

128 SIMD 16bits-PE for image processing

very similar to IMAP (NEC)

1995 — Symphonie 0,5 µm



Line processor array

256 SIMD 32bits-PE for image processing

-Network with message passing inter-PE
-Hardware acceleration of floating point operations
-16 PE multi-chip modules

2000 — Symétrie 0,25 µm

Supercomputer
Several thousands of chips

1 chip :
-10 Millions of transistors
-Reconfigurable capacities
-Fault tolerance mechanisms
- 250 MHz
- 8 W

2008 — Carvision 65 nm

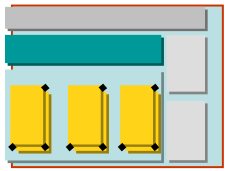
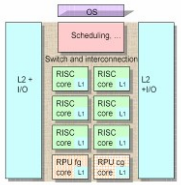


Image processor for automotive Applications
ST collaboration

- Pedestrian detec.
- Blind spot
- Lane departure
- Parking assist.

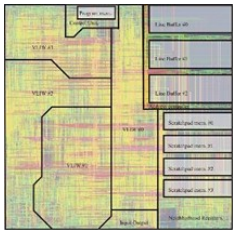
2009 — SCMP concept (MPPA, TeraOps, PTF2012)



Multicore architecture
for embedded applications

- based on SCMP CEA concepts
- 1 Tera Operations /s targeted

2010 — eISP



Processor Array
VLIW + SIMD

- low power
-Low surface
-High flexibility
-

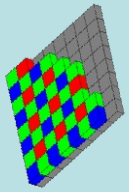
Computing for Imaging Activities at CEA LIST

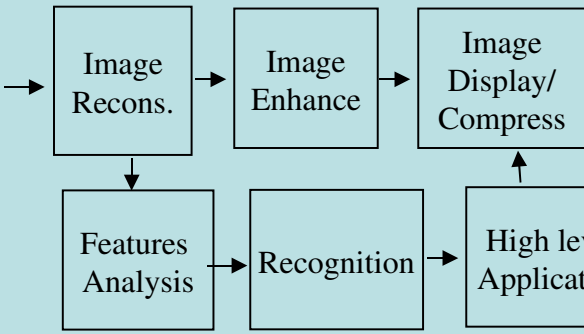
Advanced Driver Assistance System :

- **ADAS for transportation (cars, tramways, buses…)**

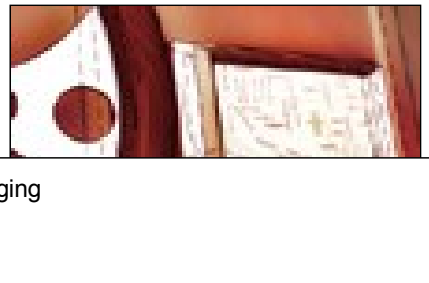
Nomadic applications (mobile phone, smart camera) :

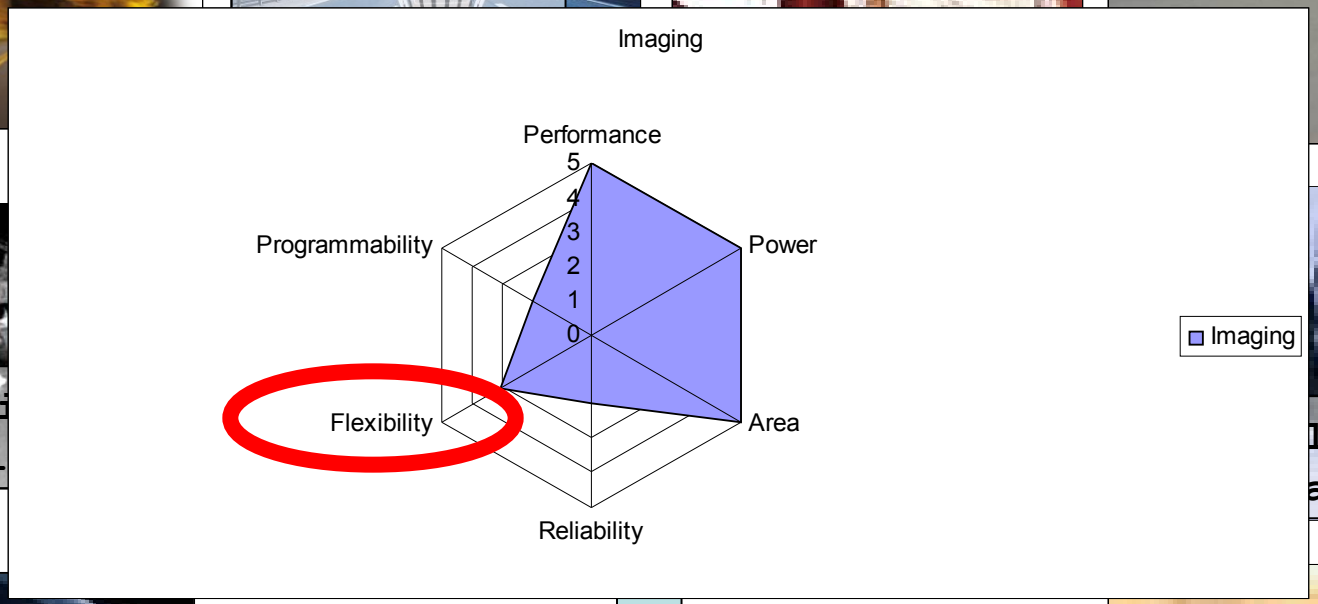
- **from image reconstruction up to feature detection/recognition**

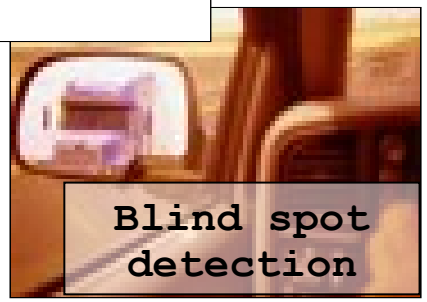




Automotive ADAS

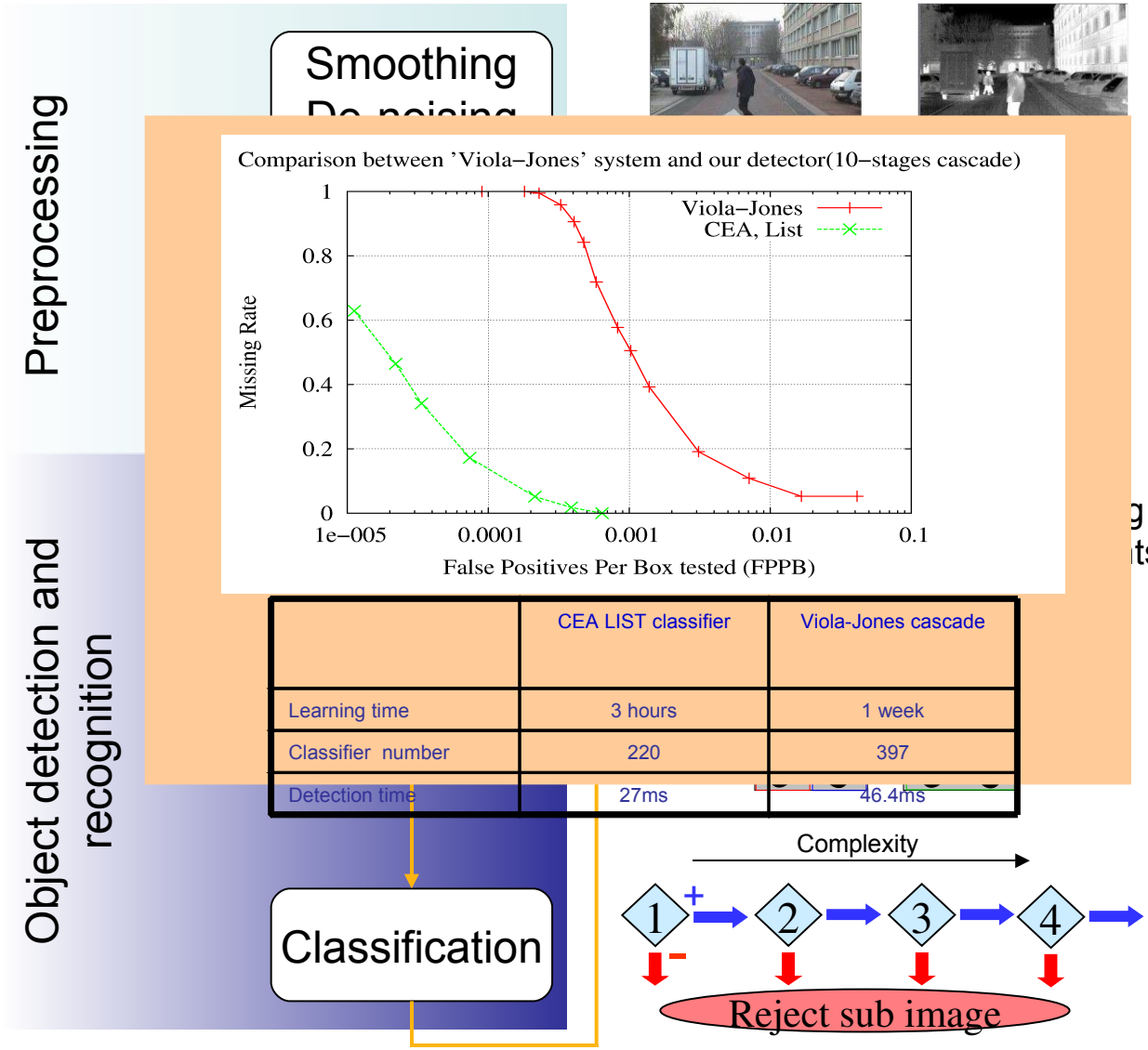




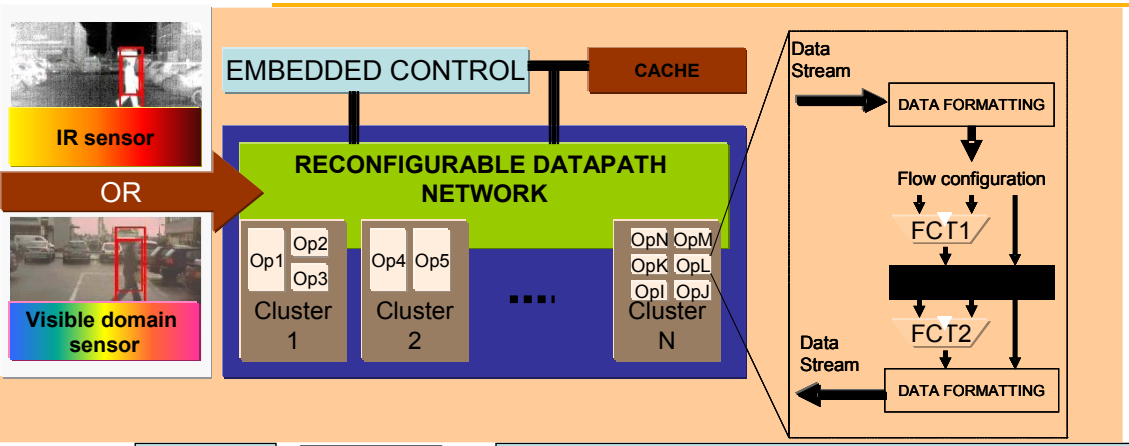


- Generic & flexible
- High computing capacity
- Silicon & power efficient

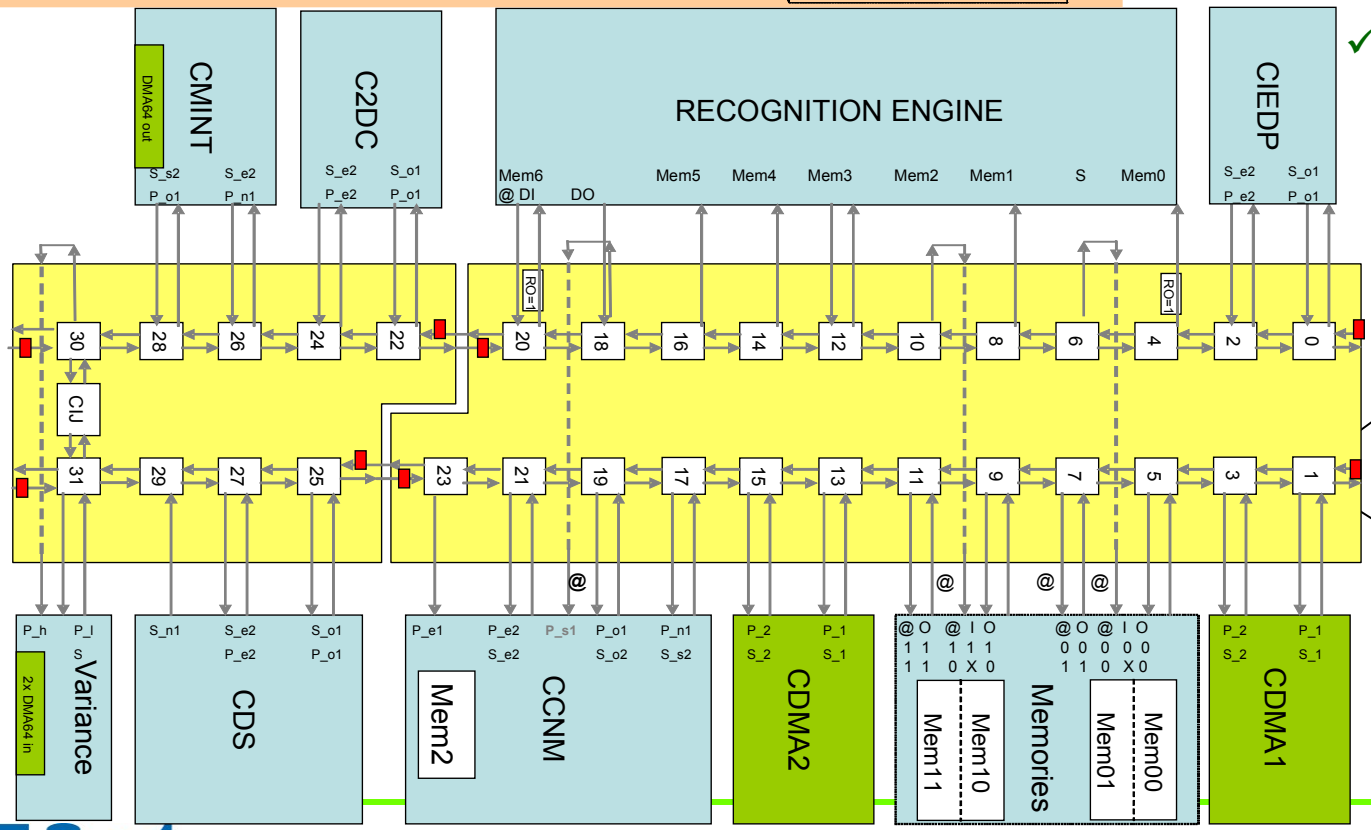
Pedestrian Detection (Pattern Matching)

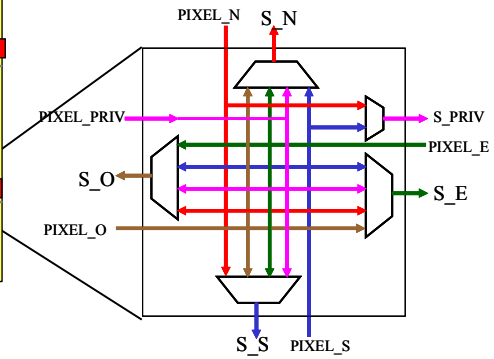


CarVision MPSoC Architecture



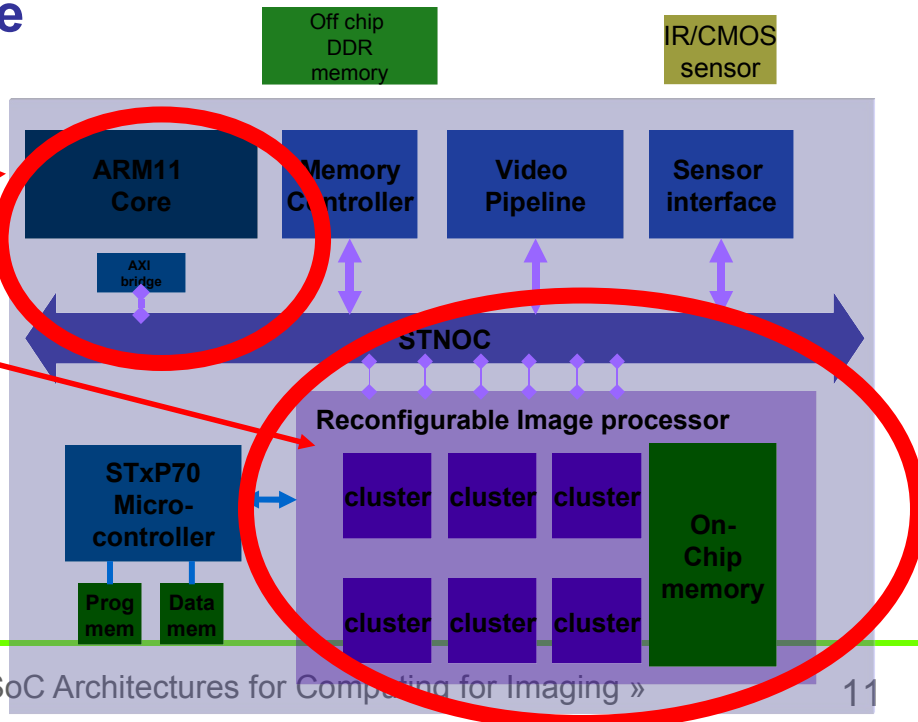
- **7 heterogeneous clusters**
  - ✓ Runtime reconfigurable
  - ✓ Low level image processing operators
  - ✓ Datapath model
- **Hierarchical cluster interconnections**
  - ✓ Allows direct chaining of operators
  - ✓ Runtime reconfigurable





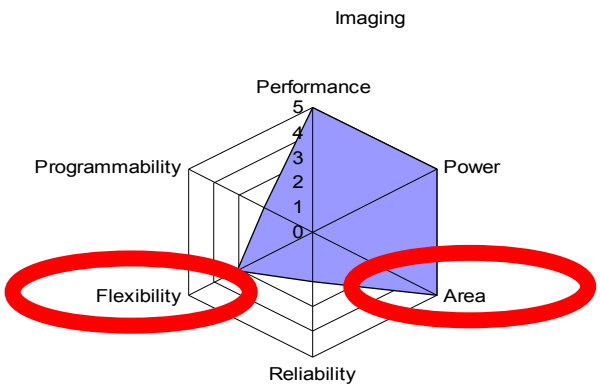
CarVision Video-Processor Overview

- Up to 50 GOPS at 200 MHz (CMOS 65nm STM)
- Reconfigurable processor able to handle pattern recognition (IR & visible spectrum)
- Area 30 mm2
  - ✓ ARM11 processor
  - ✓ 3,5 MB embedded SRAM
  - ✓ Reconfigurable Image Processor



Nomadic System Roadmap

- **Constrained by high volumes and low cost for consumer applications:**
  - ✓ **Performance needs of 100/200 GOPS for HD video**
  - ✓ **Smallest footprint (avoid image memories): surface is cost**
  - ✓ **Consumption well under 500mW**
  - ✓ **High reusability, then flexibility needs**



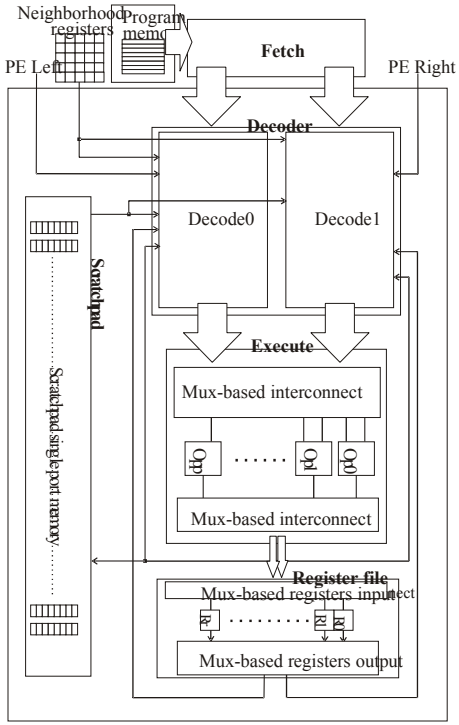
From dedicated HW
to programmable and
reconfigurable accelerators

eISP : Embedded Image Signal Processor

eISP main features :

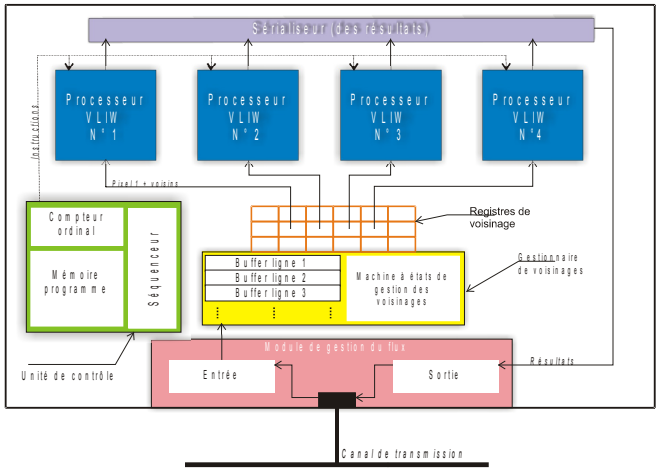
Clusters of programmable processors

- ✓ Based on a tiny VLIW processor
  - 5 kGates - 4 mW
  - 0.02 mm² area in 65nm-technology
  - 400 MIPS at 200 MHz
- ✓ SIMD clusters of processors
- ✓ Adress generation & control handled by specific units
- ✓ Configurable chaining of computing elements
- ✓ No need for the programmer to think parallel



Sizing Example for preprocessing HD Video 1080p (1920x1080 25FPS)

- ✓ 6 clusters of 6 processors
- ✓ 1,3 mm2 (memory lines included) in 65nm TSMC
- ✓ 250 mW at 200 MHZ - 14 GOPS peak



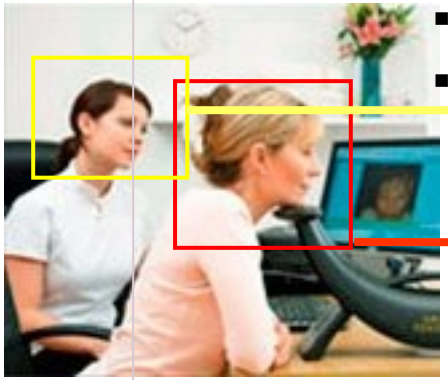
PACS : Programmable Architecture for CMOS Sensor

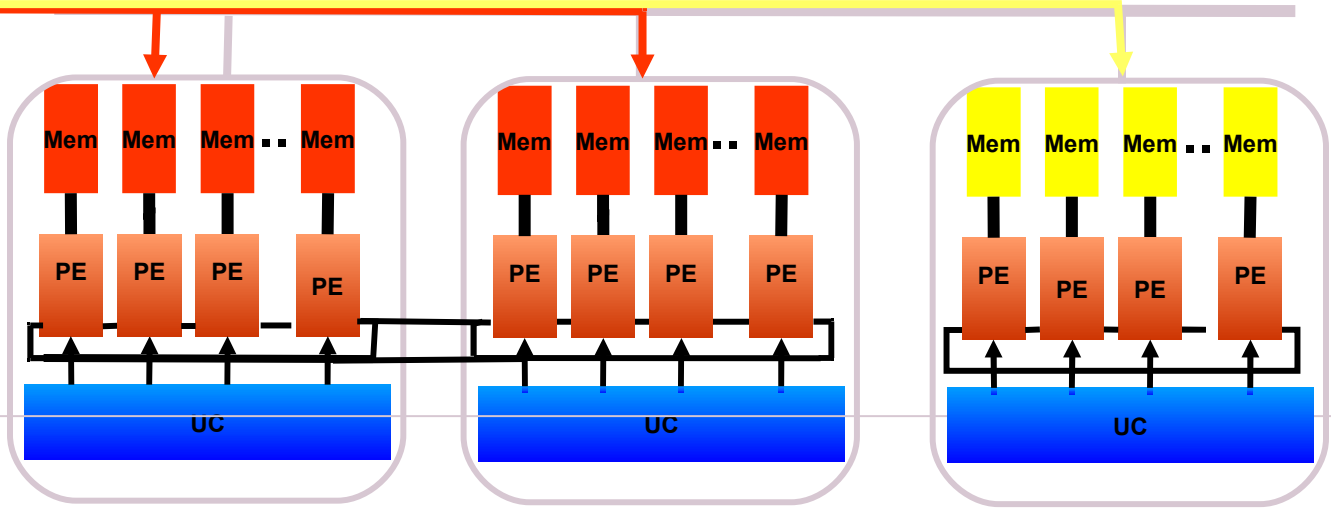
Objectives

- Taking advantage of 3D-stacking technologies to integrate both analog and digital computing resources in/near the FPA for videosurveillance applications
- Revisiting the VideoPipe

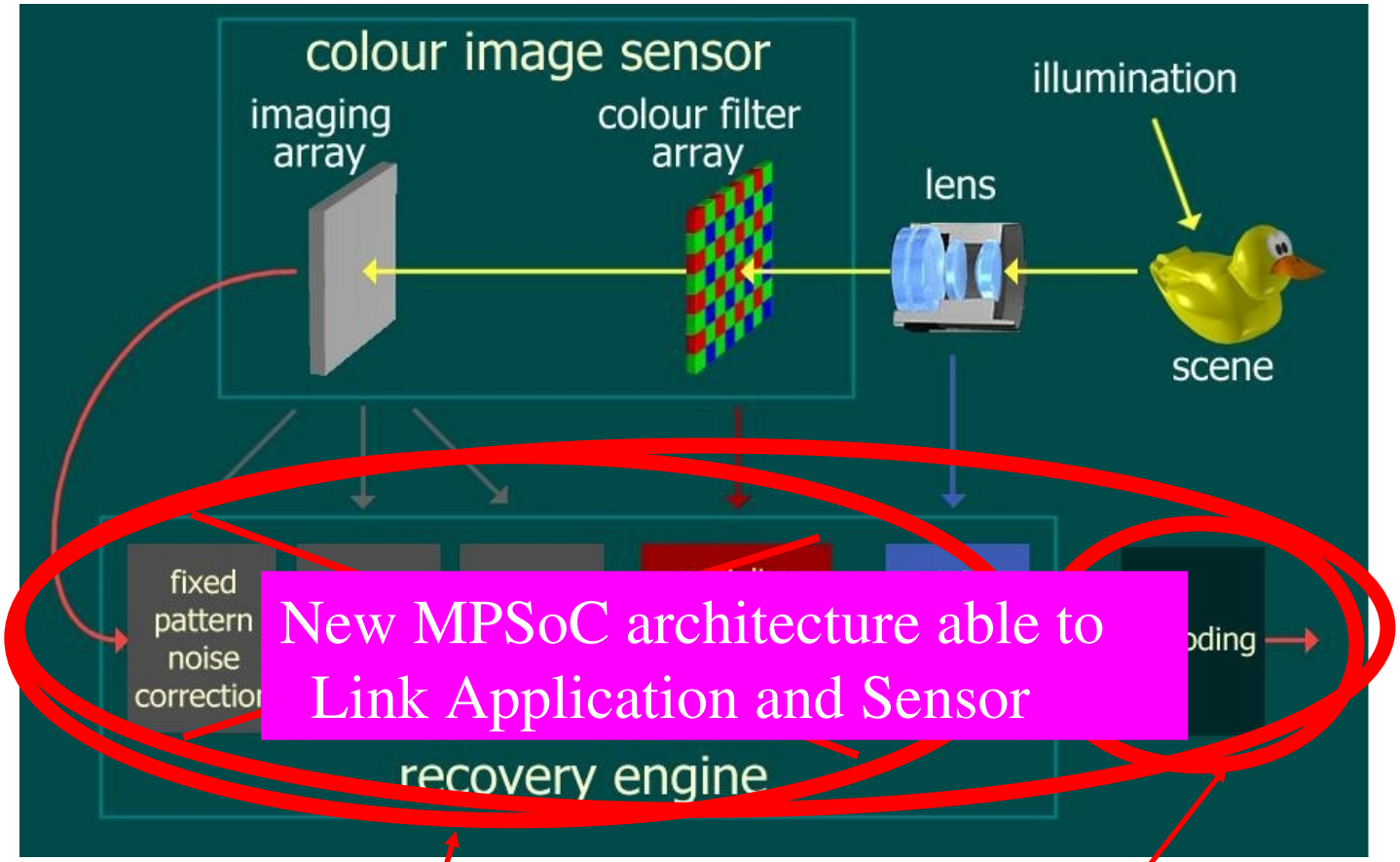
Parallel architecture behind the FPA

- SIMD clusters of processors with distributed memory banks
- Adaptation of the processing resources to the size of the ROI





Smart Imaging for Advanced Perception



Courtesy STM

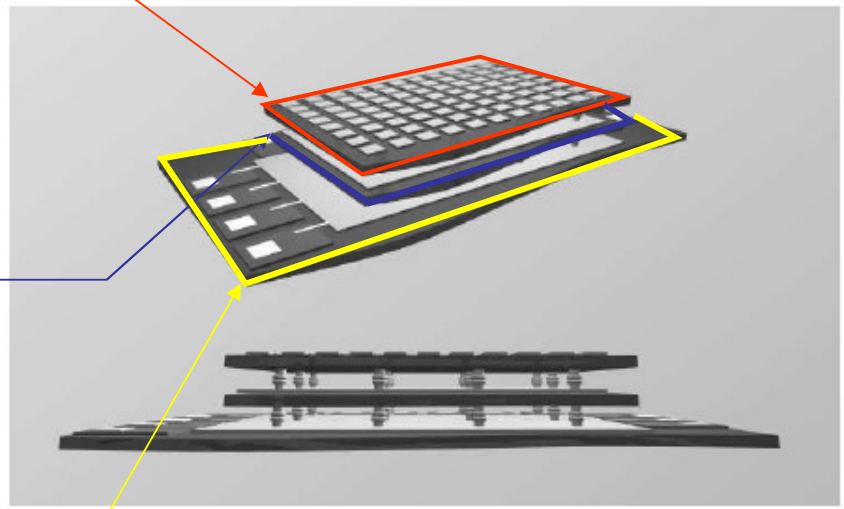
Interaction processing/pixels

+ Image processing

Future : 3D-Stacked Vision System

Sensor including analog operators and via shared between pixels

Serie of AD convertors to output several pixel flows in parallel + bio-inspired pre-processing (nanotechnology)



Digital parallel processor designed in an advanced technology

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