FINAL PROGRAM

SUNDAY JUNE 27: WELCOME

18.00 Registration

19.00 Welcome reception

MONDAY JUNE 28

8.30 Registration continued

SESSION 1: KEYNOTE

8.30 Naoki Nishi, NEC Corp., Japan

MPSoc Technology Direction in Real World Computing

9.30 Break

SESSION 2: DESIGN METHODOLOGY (MINI-KEYNOTES)

10.00 Guy Bois, Ecole Polytechnique Montréal, Canada

Fast and accurate estimation for automatic design space exploration of MPSoC systems

10.12 Frédéric Pétrot, TIMA Laboratory, INP-Grenoble, France

Annotation within dynamic binary translation for fast and accurate system simulation

10.24 Norbert Wehn, University of Kaiserslautern, Germany

Efficiency Metrics for Design Space Exploration of Wireless Baseband Processing

10.36 Ahmed Jerraya, CEA-LETI, France

How can MPSoC take benefit from emerging 3D-IC technology?

10.48 Vijaykrishnan Narayanan, Pennsylvania State University, USA

Influence of emerging device technologies on system design

11.00 El Mostapha Aboulhamid, Universite de montreal, Canada

Timing verification of subsystems integration

11.12 Suzanne Lesecq, CEA LETI MINATEC, France

Robust control of a FLL

11.24 Panel with the lecturers (for Session 1 and 2)

12.30 Lunch

SESSION 3: DOMAIN SPECIFIC PROCESSING (IN-DEPTH TECHNICAL PRESENTATIONS)

14.00 Ping Chao and Youn-Long Lin, National Tsing Hua University, Taiwan

Memory Access Optimization for Ultra High Resolution Video Decoding

14.30 Emil Matus, Technical University Dresden, Germany

MPSoC architectures for baseband signal processing of future mobile terminals

15.00 Zhiyi Yu, Fudan University, China

Pushing many-core processors as powerful and energy-efficient as ASIC for domain-specific applications

15.30 Break

SESSION 4: HW/SW INTERACTION (IN-DEPTH TECHNICAL PRESENTATIONS)

16.00 Takahisa Suzuki, Fujitsu Laboratories LTD. , Japan

System impact caused by software-hardware harmonized implementation

16.30 David Kleidermacher, Green Hills Software, USA

Multicore Virtualization for ARM Processors

17.00 Chong-Min Kyung, KAIST, Korea

Power and Temperature-Aware Clock Frequency and Thread Assignment in Multi-layer MPSoC

17.30 Panel with the lecturers (for Session 3 and 4)

19.00 Diner

TUESDAY JUNE 29

SESSION 5: KEYNOTE

8.30 Kazuo Kajimoto, Panasonic Corporation, Japan

State Transition of Software Innovation in relation to Hardware Innovation - Once was "Follower", through "Leader", it would be "Constraint" -

9.30 Break

SESSION 6: MPSOC PLATFORM (MINI-KEYNOTES)

10.00 David Atienza, EPFL, Swizerland

Active Cooling Control for Thermal Management of 3D MPSoCs

10.12 Soo-lk Chae, Seoul National University, Korea

A multi-core platform with three video-specific processsors for HD video codec applications

10.24 Jenq-Kuen Lee, National Tsing-Hua University, Taiwan

Parallelization of Stereo Vision Applications on Embedded Multi-Core Platforms

10.36 John Goodacre, ARM, UK

Extending the ARM Architecture

10.48 Chris Rowen, Tensilica, USA

Silicon-Efficient DSPs and Digital Architecture for LTE Baseband

11.00 Yuan Xie, Pennsylvania State University, USA

Modeling, Architecture, and Applications of Emerging Memory technologies for MPSOC

11.12 Rolf Ernst, Technical University of Braunschweig, Germany

Certification of Trusted MpSoC Platforms

11.30 Panel with the lecturers (for Session 6)

12.30 Lunch

SESSION 7: PROGRAMMING AND SCHEDULING (IN-DEPTH TECHNICAL PRESENTATIONS)

14.00 Martti Forsell, VTT, Finland

Strong programming models for MP-SOCs

14.30 Kees Vissers, Xilinx, USA

Programming and Performance of FPGAs all in C and C++

15.00 Martin Schoeberl, Technical University of Denmark, Denmark

Schedule Memory Access, not Threads

15.30 Break

SESSION 8: LOW POWER (IN-DEPTH TECHNICAL PRESENTATIONS)

16.00 Kunio Uchiyama, Hitachi, Ltd., Japan
Power-efficient Heterogeneous Multicore for Digital Convergence

16.30 Yasuhiro Tawara, Renesas Technology Corp., Japan
DVFS and power-off controls on a multicore operating system

17.00 Tuomas Jarvinen, ST-Ericsson, Finland
Designing for low power in SoC projects

17.30 Panel with the lecturers (for Session 7 and 8)

18.30 Speaker's Meeting

19.00 Diner

WEDNESDAY JUNE 30

SESSION 9: KEYNOTE

8.30 Marco Cornero, ST-Ericsson, Italy
MPSoc's in Mobile phones: parallel computing for the masses

9.30 Break

SESSION 10: NOC & MANY-CORE (MINI-KEYNOTE)

10.00 Marcello Coppola, STMicroelectronics, France
NoC: Myth or Reality?

10.12 K. Charles Janac, Arteris Inc., USA
Network on Chip - Not just for Complex SoCs Anymore

10.24 Gabriela Nicolescu, Ecole Polytechnique de Montréal, Canada
Multi-Objective Design Space Exploration for MPSoC

10.36 Omar Hammami, ENSTA PARISTECH, France
Design and Implementation of a NOC Based 2048 PE on Large Scale Emulator

10.48 Sungjoo Yoo, POSTECH, Korea
Network awareness in memory controllers for many-core

11.00 Panel with the lecturers (for Session 10)

12.00 Lunch

SESSION 11: KEYNOTES

13.30 Sebastian Steibl, Intel, Germany
Single-chip Cloud Computer: Architecture, Design and Application of a 48 Core Research Microprocessor

SESSION 12: HETEROGENEOUS MPSOCS (IN-DEPTH TECHNICAL PRESENTATIONS)

14.30 Yankin Tanurhan, Virage Logic, USA
Seamless Integration of Heterogeneous Co-Processors in Today's SoCs

15.00 Sri Parameswaran, University of New South Wales, Australia
Heterogeneous Multi-Processor Pipelines: an MPSoC Story

15.30 Break

SESSION 13: APPLICATIONS (IN-DEPTH TECHNICAL PRESENTATIONS)

16.00 Rudy Lauwereins, IMEC, Belgium
Processors for wireless sensor nodes: can you do something useful in just a few microwatts

16.30 Kees van Berkel, STEricsson, Eindhoven University of Technology, France
Multi-Core for Mobile Phones

17.00 Yukoh Matsumoto, TOPS Systems Corporation, Japan
CG Application Domain Specific Heterogeneous Multi-Core Processor

17.30 Panel with the lecturers (for Session 12 and 13)

19.00 Banquet

THURSDAY JULY 1

SESSION 14: KEYNOTE

8.30 Pieter J. Mosterman, MathWorks, USA
A computational semantics of time-based models and its role in Model-Based Design

9.30 Break

SESSION 15: HW & SW TECHNIQUES (MINI-KEYNOTE)

10.00 Ulrich Ramacher, Infineon, Germany
On the Challenges of Programming XGOLD SDR 20

10.12 Raphaël David, CEA LIST, France
Low Power management in embedded multi-core architectures

10.24 Kees Goossens, Eindhoven University of Technology, Netherlands
Virtualized Processor Power Management

10.36 Joachim Kunkel, Synopsys, USA
Virtual Prototyping : Reality for Prime Time?

10.48 Kiyoung Choi, Seoul National University, Korea
Some Applications of Coarse-Grained Reconfigurable Array

11.00 Lars Bauer, Karlsruhe Institute of Technology, Germany
KAHRISMA: A Multi-grained Reconfigurable Multicore Architecture

11.12 Pieter Van der Wolf, Virage Logic, Netherlands
Efficient and predictable integration of MPSoCs

11.30 Panel with the lecturers (for Session 15)

12.30 Lunch

SESSION 16: NOC (IN-DEPTH TECHNICAL PRESENTATIONS)

14.00 Yuichi Nakamura, NEC Corp., Japan
The layout evaluation and hierarchical layout method of NoCs

14.30 Takashi Miyamori, Toshiba Corporation, Japan
Evaluation of Network-on-Chip for Large Scale Many-Core Systems

15.00 Ian O'connor, Lyon Institute of Nanotechnology, France
Optical networks on chip for MPSoC data communication

15.30 Panel with the lecturers (for Session 16)

17.45 Dinner (w/ cruise watching cormorant fishing)

FRIDAY JULY 2

SESSION 17: KEYNOTE

8.30 Jae Cheol Son, Samsung Electronics, Korea
MPSoC Technology for New Wave of User Experiences

9.30 Break

SESSION 18: EMERGING DEVICE AND DESIGN TECHNOLOGIES (MINI-KEYNOTES)

10.00 Koichiro Yamashita, Fujitsu Laboratories LTD., Japan
Evaluation and development methodology for progressing of MPSoC technology to industrial field of mobile platform

10.12 Tsuyoshi Isshiki, Tokyo Institute of Technology, Japan
MPSoC Platform for Super Hi-vision Video Processing System

10.24 Benjamin Carrion Schafer, NEC Corp., Japan
Complete C-Based SoC Design: Is it possible?

10.36 Jan Madsen, Technical University of Denmark, Denmark
A Bio-Inspired Reconfigurable Hardware Architecture Supporting Self-organisation and Self-healing

10.48 Break

SESSION 19: 3D-IC TECHNOLOGIES (IN-DEPTH TECHNICAL PRESENTATIONS)

11.00 Tadahiro Kuroda, Keio University, Japan
ThruChip Interface (TCI) for 3D System Integration

11.30 Hsien-Hsin Sean Lee, Georgia Institute of Technology, USA
Design, implementation, and test for a 3D-IC many-core processor

12.00 Panel with the lecturers (for Session 18 and 19)

13.00 Lunch

Further information: *http://www.mpsoc-forum.org/*