FINAL PROGRAM

SUNDAY JULY 3: WELCOME

18:00 Registration

19:00 Welcome reception

MONDAY JULY 4

8:30 Registration continued

SESSION 1: KEYNOTE

8:30 Kerry Bernstein, IBM, USA
Architectural Directions for Future Nanoscale Computing Systems

9:30 Break

SESSION 2: MEMORY/CACHE/STORAGE

10:00 Sungjoo Yoo, POSTECH, Korea
Low power hybrid PRAM/DRAM main memory

10:12 Hsien-Hsin Sean Lee, Georgia Institute of Technology, USA
Toward the design of robust and self-healing memories

10:24 Hiroyuki Tomiyama, Ritsumeikan University, Japan
Challenges of Programming Embedded Many-Core SoCs with OpenCL

10:36 David Kleidermacher, Green Hills Software, USA
Multicore Virtualization Update

10:48 Raphaël David, CEA LIST, France
Hardware support for online resources management

11:00 Soo-lk Chae, Seoul National University, Korea
Optimization of an H.264 decoder using its communication-centric model

11:12 Panel with the lecturers (for Sessions 1 and 2)

12:30 Lunch

SESSION 3: HIGH PERFORMANCE COMPUTING

14:00 Dongrui Fan, Chinese Academy of Science, China
Godson-T: A High-Efficient Many-Core Architecture for Parallel Program Executions

14:30 Paolo Faraboschi, HP Labs, Spain
System-Level Integration for Scale-out Computing

15 :00 Patrick Blouet, ST Ericsson, France
Mobile cloud computing

15:30 Break

SESSION 4: CONTINUING MOORE'S LAW

16:00 John Goodacre, ARM, UK
Understanding what those 250 million transistors are doing

16:30 Michael Chang, Global Unichip, Taiwan
28nm Dual Core SoC

17:00 Panel with the lecturers (for Sessions 3 and 4)

19:30 Diner

TUESDAY JULY 5

SESSION 5: KEYNOTE

8:30 Bing Sheu, Director of R&D, TSMC, Taiwan
Design Technology for Future Computing Systems

9:30 Break

SESSION 6: 3D IC

10:00 Koji Inoue, Kyushu University, Japan
Adaptive Execution on 3D Microprocessors

10:30 Yukoh Matsumoto, TOPS Systems Corporation, Japan
COOL System: Low-Power 3-D Heterogeneous Multi-Core/Multi-Chip Architecture

10:42 David Atienza, EPFL, Swizerland
System-Level Thermal Management of 3D MPSoCs with Active Cooling

10:54 Yuan Xie, Penn State, USA
Memory-Stacking for Future High-Performance Microprocessor

11:06 Ahmed Jerraya, CEA LETI, France
3D-IC for Computing

11:18 Panel with the lecturers (for Sessions 5 and 6)

12:30 Lunch

SESSION 7: POWER/ENERGY

14:00 Tohru Ishihara, Kyushu University, Japan
Energy Characterization of Embedded Processors for Software Energy Optimization

14:30 Yoshinori Takeuchi, Osaka University, Japan
Task Assignment Method for DVS based multiprocessor SoC

15:00 Edith Beigné, CEA LETI, France
Fine-grain DVFS power-aware control

15:12 Youn-Long Lin, National Tsing Hua University, Taiwan
Multiprocessor Scheduling taking into account Energy Harvesting and Storage

15:24 Break

SESSION 8: SOFTWARE

16:00 Yuichi Nakamura, NEC, Japan
A software development toolset for multi-core processors

16:12 Emil Matus, Technical University Dresden, Germany
Benchmarking of Dataflow Programming Models for MPSoC

16:24 Jenq-Kuen Lee, National Tsing Hua University, Taiwan
Support of C++ Compiler for Embedded Multi-Core DSP Systems

16:30 Panel with the lecturers (for Sessions 7 and 8)

20:15 Diner

WEDNESDAY JULY 6

SESSION 9: KEYNOTE

8:30 Alain Artieri, VP of ST Ericsson, France
Technical challenges to be in the race of the exploding Smartphone and Tablet market

9:30 Break

SESSION 10: MOBILE PLATFORM

10:00 Ruchir Puri, IBM, USA
Design and CAD challenges: 22nm and beyond

10:30 Lasse Harju, ST Ericsson, France
Sensor processing and power management in smartphone platforms

11:00 Rudy Lauwereins, IMEC, Belgium
BOADRES: a scalable baseband processor template for Gbps radios

11:12 Kees van Berkel, STEricsson, Eindhoven Univ., The Netherlands
Multicore for 4G:3GP versus.

11:24 Chris Rowen, Tensilica, USA
Design of a 100GMAC/sec DSP Core for 4G Wireless

11:36 Yankin Tanurhan, Synopsys, USA
MPSoC Subsystems: A New Reuse Paradigm

11:48 Panel with the lecturers (for Sessions 9 and 10)

12:30 Lunch

SESSION 11: MULTICORE ARCHITECTURE

14:00 Martin Schoeberl, Technical University of Denmark, Denmark
A Time-predictable Microprocessor: the Patmos Approach

14:12 Kees Goossens, Eindhoven University of Technology, The Netherlands
Architecture Requirements for Composability and Predictability

14:24 Martti Forsell, VTT, Finland
MCPA - MultiCore Portability Abstraction

14:36 Charles Janac, Arteris InC. USA
Interchip Link Technology

14:48 Gerhard P. Fettweis, TU Dresden, Germany
Exploration of NoC Design & Management Concepts for MPSoC

15:00 Marcello Coppola, ST, France
SoC interconnect: Current Challenges and Future Directions.

15:12 Pieter van der Wolf, Synopsys, The Netherlands
Audio Subsystem Solutions for Consumer SoCs

15:24 Drew Wingard, Sonics, USA
TBD

15:36 Panel with the lecturers (for Session 11)

16:25 Break

16:45 Speaker's Meeting

18:15 Bus departure to Chateau Clos Vougeot

THURSDAY JULY 7

SESSION 12: KEYNOTE

8:30 Kasahara Hironori, Wasada Univ., Japan
Homogeneous and Heterogeneous Multicore / Manycore Processors, Parallelizing Compiler and Multiplatform API for Green Computing

9:30 Break

SESSION 13: RECONFIGURABLE ARCHITECTURE

10:00 Paul Heysters, Recore systems, The Netherlands
A Glimpse into Future Reconfigurable Many-cores for Embedded Stream Processing

10:30 Kees Vissers, Xilinx, USA
Programming for performance in FPGAs using multiple processors and accelerators with C/C++ programming

11:00 Kiyoung Choi, Seoul National University, Korea
Transparent Binary Acceleration using Reconfigurable Array

11:12 Ian O'connor, Lyon Institute of Nanotechnology, France
Nanofabrics for reconfigurable computing cores

11:24 Omar Hammami, ENSTA PARISTECH, France
MPSOC Synthesis: Combining NOC Synthesis with Multiobjective Design Space Exploration on Large Scale Emulator

11:36 Panel with the lecturers (for Sessions 12 and 13)

12:30 Lunch

SESSION 14: ARCHITECTURE

14:00 Kunio Uchiyama, Hitachi, Ltd., Japan
Heterogeneous Multicore Processor Technologies for Embedded Systems

14:30 Pierre Paulin, ST, Canada
Exploring H/W and S/W solutions to MP-SOC platform mapping: An Industrial Perspective

15:00 Nakajima Masaitsu, Panasonic, Japan
Next Generation Multi-Processor Architecture for "Network Era UniPhier"

15:30 Norbert When, University of Kaiserslautern, Germany
Hardware Accelerators for Financial Mathematics - Methodology, Results and Benchmarks

15:42 Takashi Miyamori, Toshiba, Japan
Heterogeneous Multi &Many Core Processors for Multimedia Applications

15:54 Tsuyoshi Isshiki, Tokyo Institute of Technology, Japan
Trace-Driven Workload and Bus Traffic Simulation for MPSoC Architecture Evaluation

16:06 break

16:15 Panel with the lecturers (for Session 14)

20:00 Dinner

FRIDAY JULY 8

SESSION 15: KEYNOTE

8:30 Philippe Magarshack, VP of ST-Microelectronics, France
Gaining 10x in power efficiency in the next Decade in Consumer Products

9:30 Break

SESSION 16: METHODOLOGIES FOR MPSOC

10:00 Bart Kienhuis, Compaan Design, The Netherlands
Using C-to-Dataflow for portable and efficient mapping on Heterogeneous MultiCore designs

10:12 Joachim Kunkel, Synopsys, USA
TBD

10:24 Rolf Ernst, Technical University of Braunschweig, Germany
MPSoC for safety critical applications – from multicore to manycore

10:36 Frédéric Pétrot, TIMA Laboratory, INP-Grenoble, France
An analytical model for Many-Functionally Asymmetric Core SoC Architectures

10:48 Sri Parameswaran, University of New South Wales, Australia
Security and Reliability in an MPSoC environment

11:00 Ryoichi Yamashita, Fujitsu, Japan
A software centric system design for OS scheduling scheme in the upstream phase

11:12 Panel with the lecturers (for Sessions 15 and 16)

12:30 Lunch