Introduction to BaseBandEngine 64

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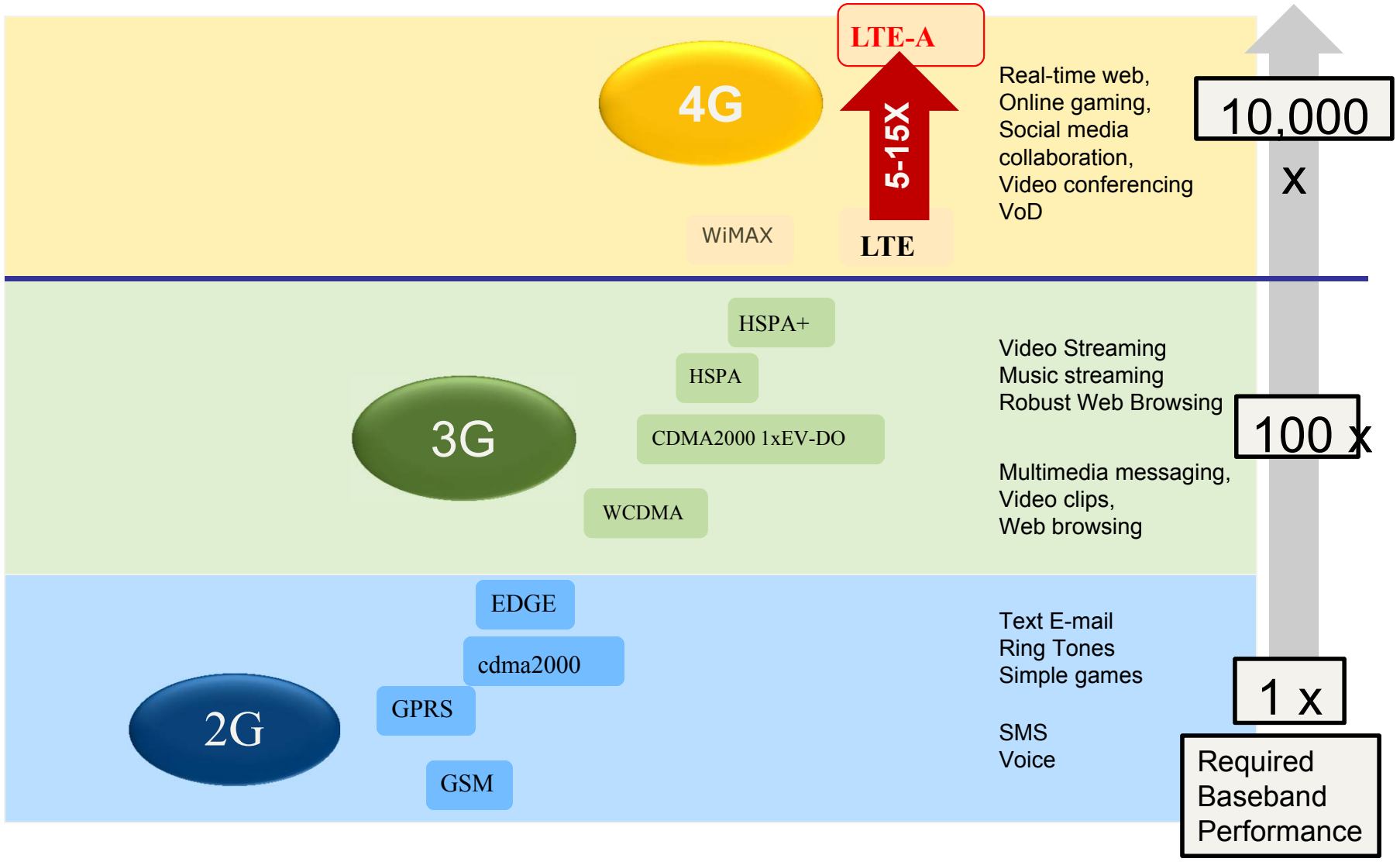
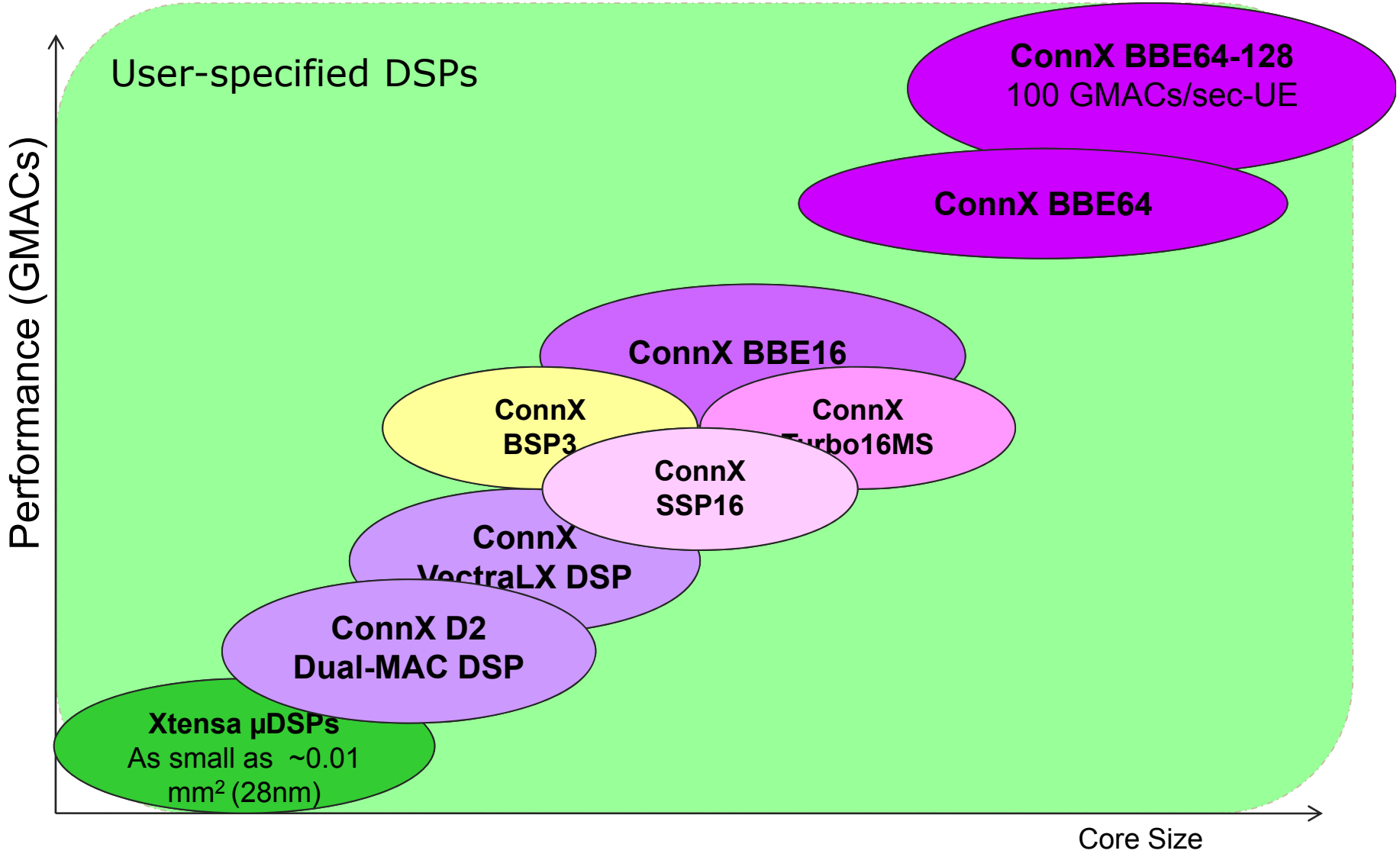
July 2011

Why BBE64? 4G Wireless, especially LTE-Advanced

Quantum Step in Required Performance

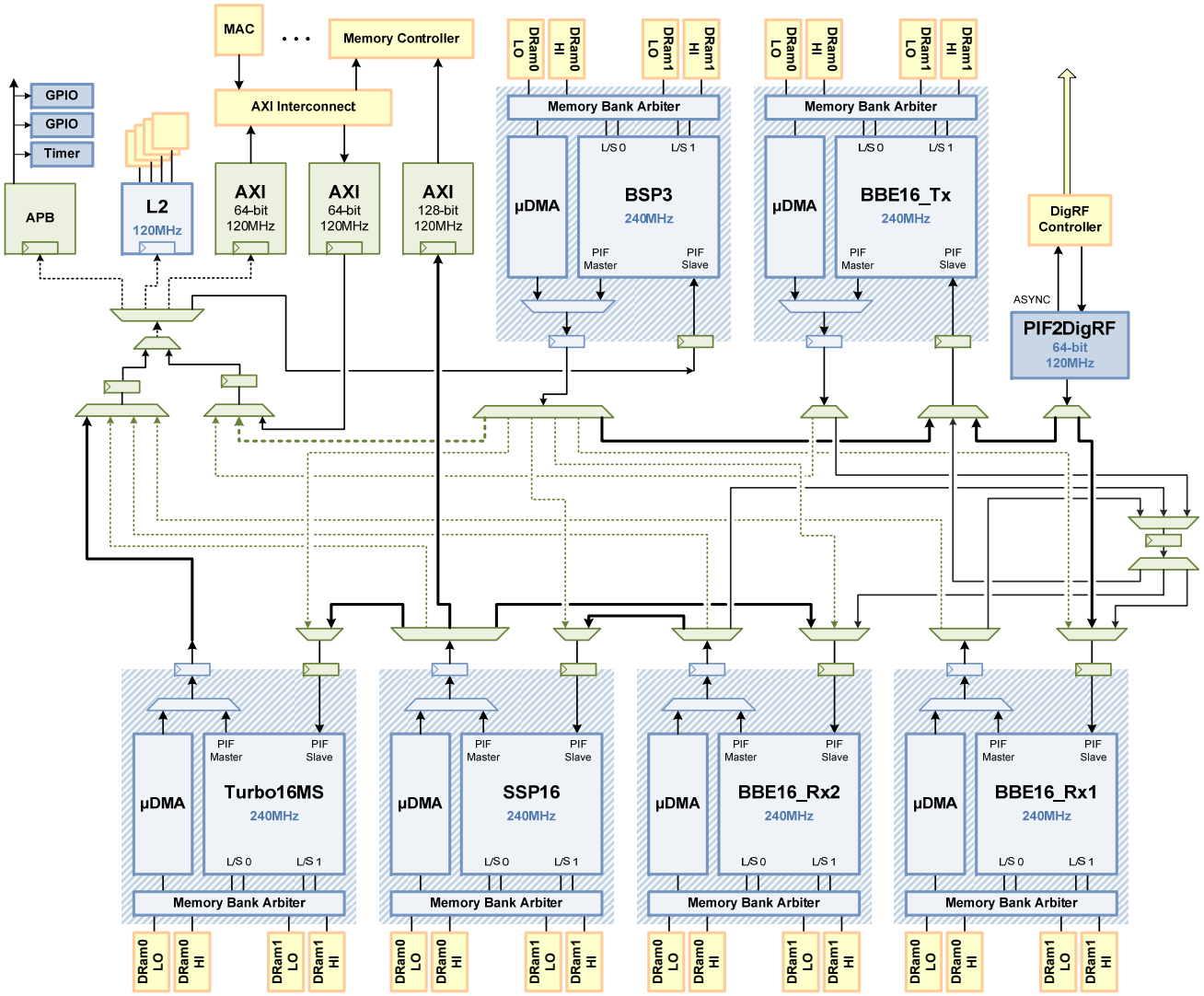


Tensilica Meets a Breadth of DSP Design Requirements

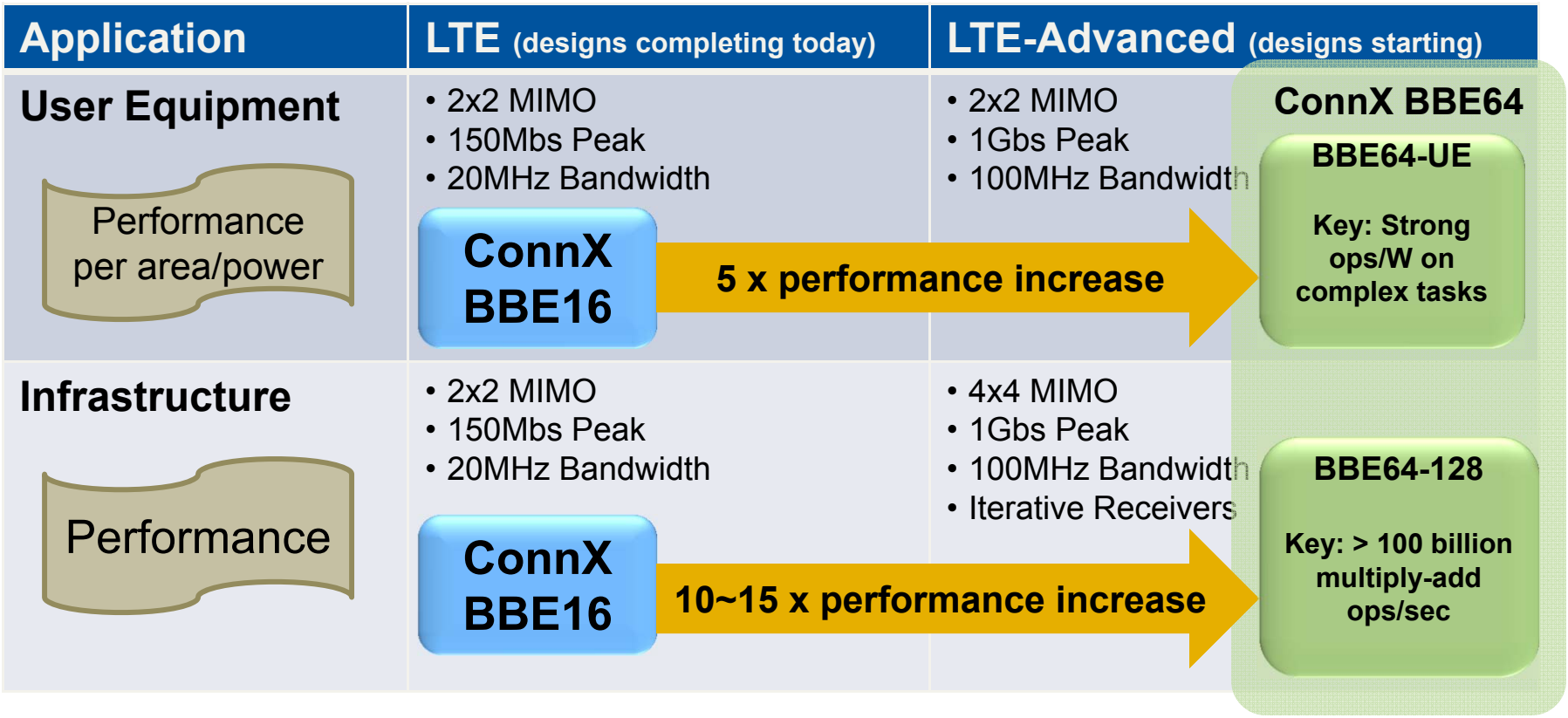


Atlas System Block Diagram

Fully Software Programmable LTE Cat4 Reference Design



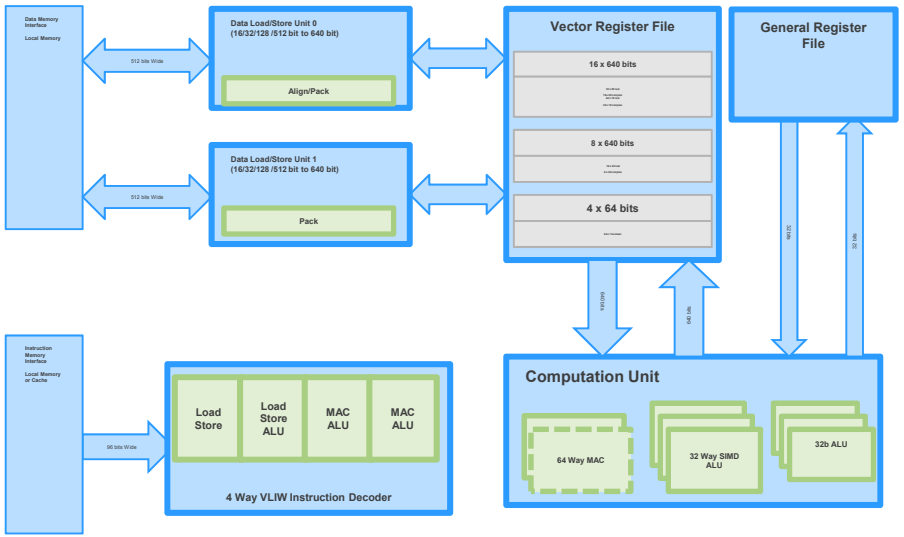
DSP Computation Requirements of LTE Advanced



A range of solutions is required to meet the needs of LTE Advanced

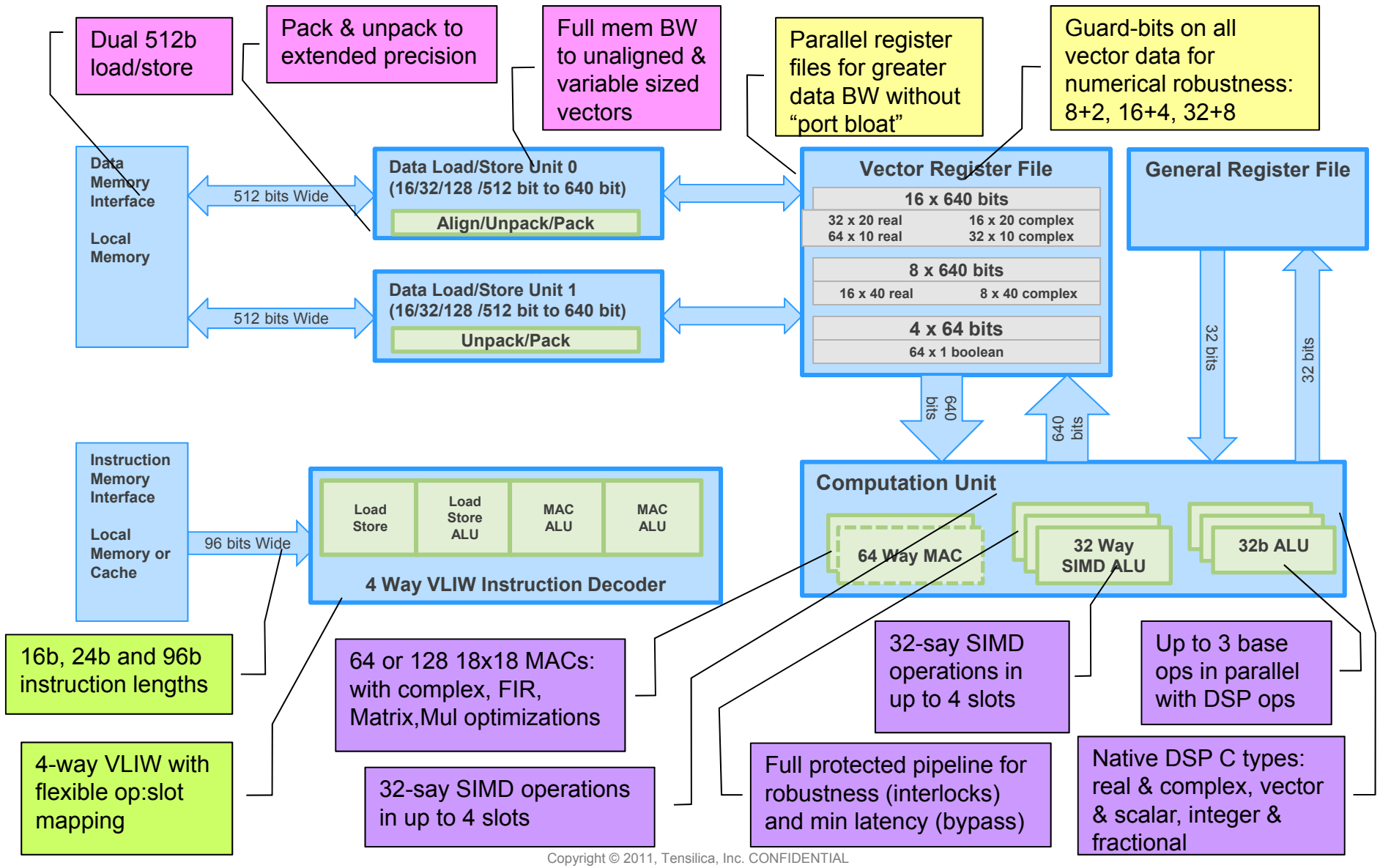
BBE64 Family Design Goals and Philosophy

- World-leading DSP performance for baseband PHY in terminals and infrastructure
- Combine SIMD, VLIW and configurable instruction set features for large applications “sweet-spot”.
- Leverage extremely high memory system bandwidth of Xtensa LX4 – 1024b per cycle

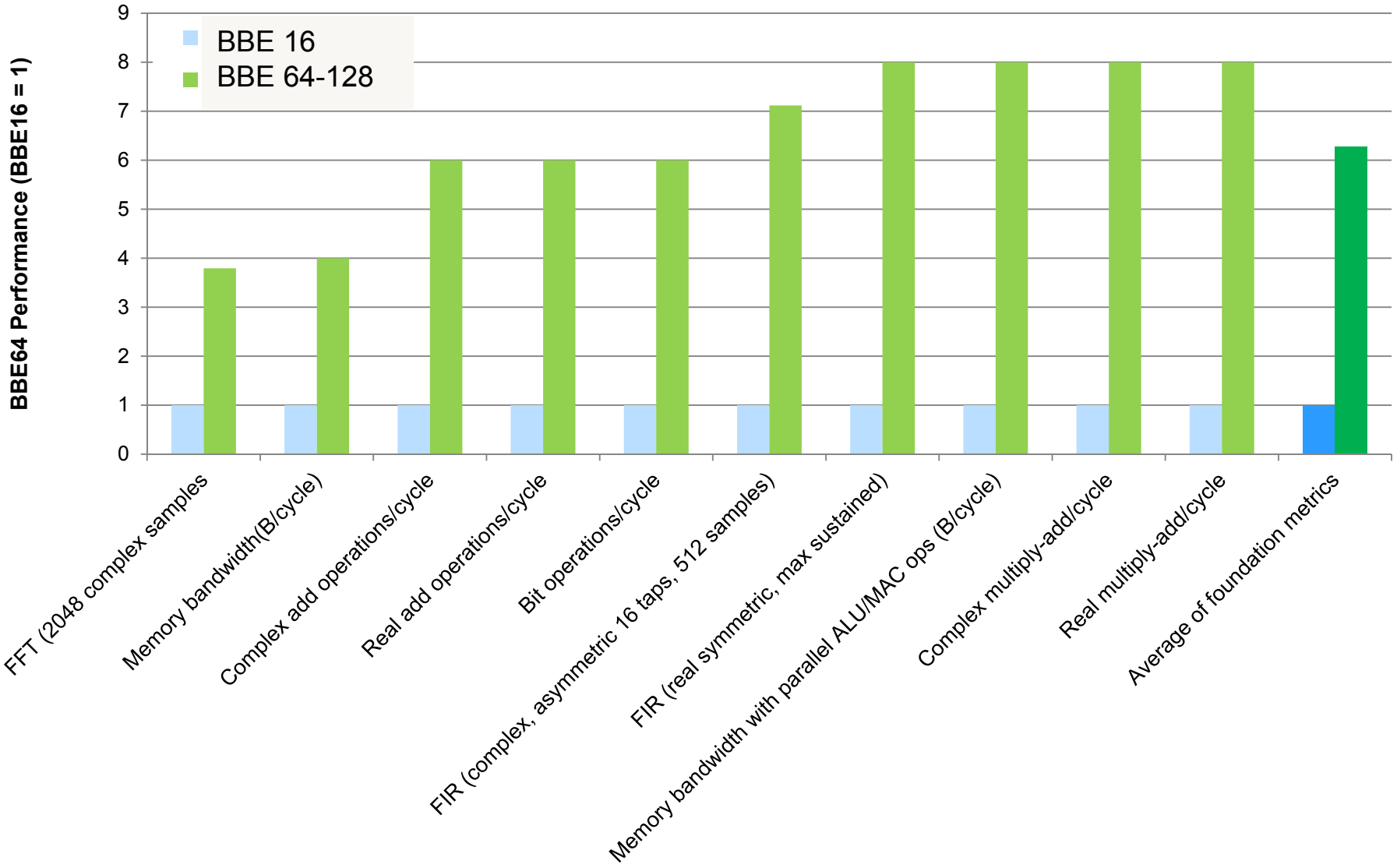


- Boost control code performance with multi-issue base ops
- Leverage state-of-the-art vectorizing compilers, C scalar/vector data-types, operator-overloading and optimized intrinsics to eliminate need for assembly
- Full ConnX BBE16upward compatibility
- Fully synthesizable RTL, with complete system modeling, verification and back-end flows environment
- Register-file port and instruction packing optimizations to minimize area/power
- Foundation for further customer optimization by configuration and TIE

ConnX BBE64 – for LTE Advanced

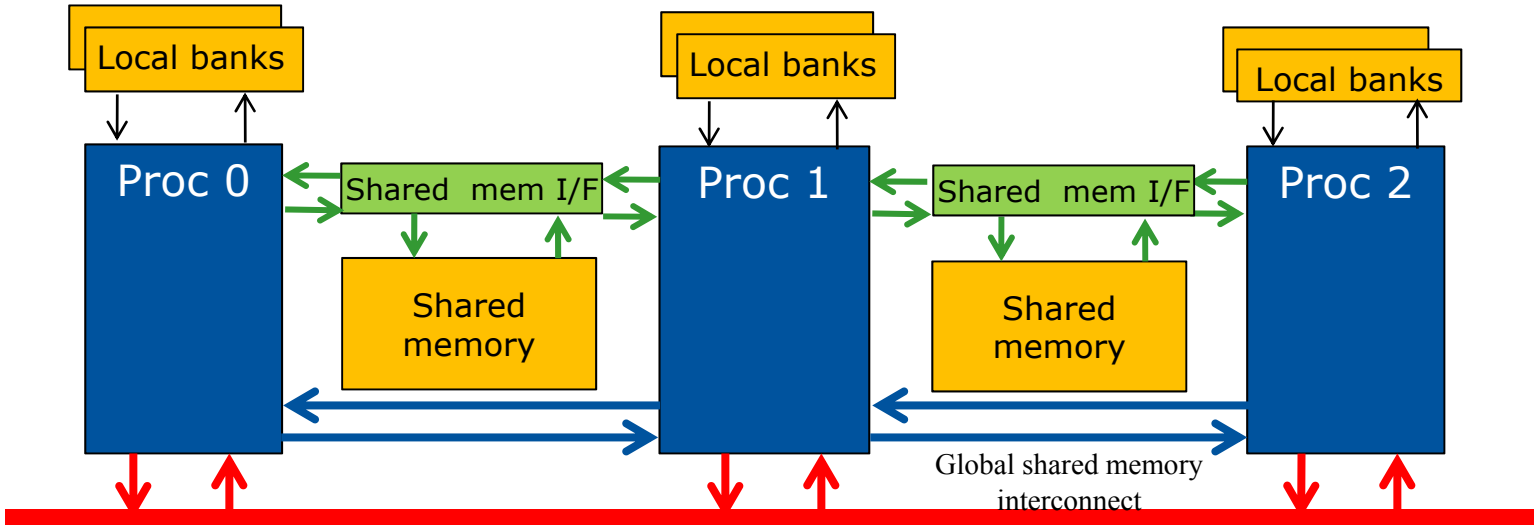


Performance Boost for LTE Advanced



BBE64 Connectivity in Wireless Baseband Systems

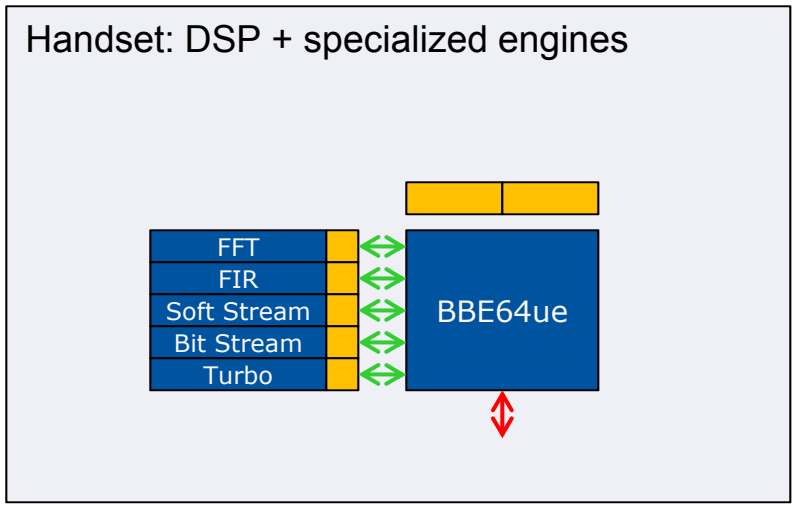
Three complementary processor-processor interconnect types

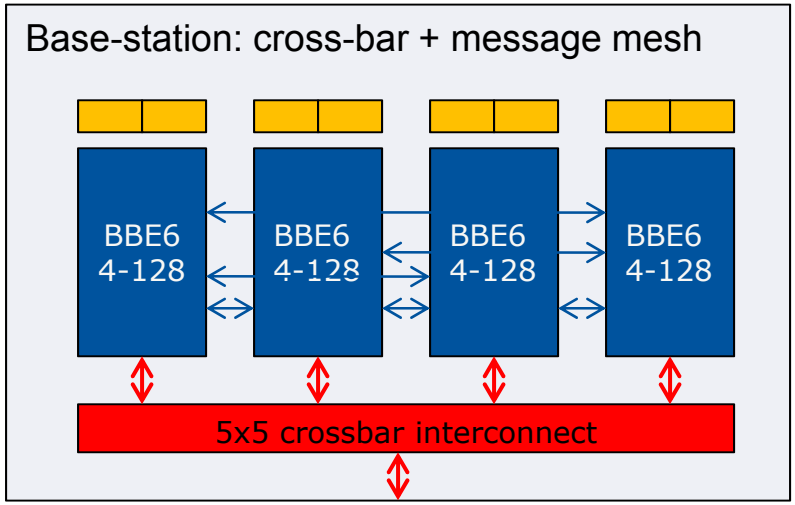


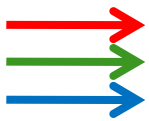
Streaming links to global shared memory interconnect @ 13GB/s: [up to 1 per processor]
Streaming links to locally shared memory @ >50GB/s: [up to 2 per processor]
Streaming data and control queues @ >64GB/s: [up to 4 per processor]

New Directions in DSP Memory Systems

- Two or more wide memory operations per cycle
- Full bandwidth on unaligned data streams
- High-efficiency, tightly-coupled DMA support to/from local data memory
- Multiple references per cycle to data cache
- Direct connect data queues: blocking/non-blocking
- DSP data cache coherency – possible, but is it an efficient approach?







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