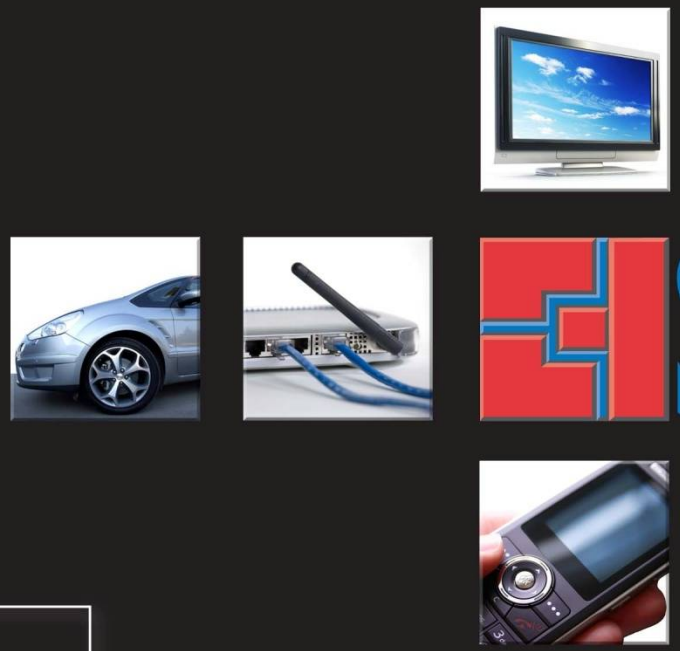


SONICS

Leveraging Multichannel 3D DRAMs in MPSoCs

Drew Wingard, Sonics

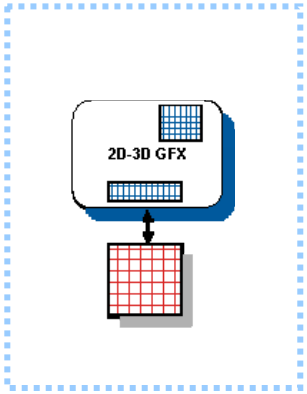
From MPSoC '06: NoC is the Answer! (What was the Question?)

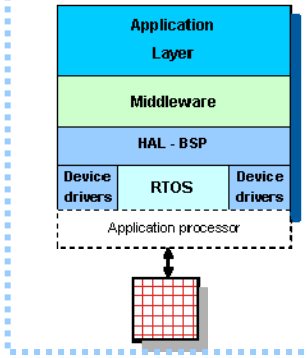
NoC Myths

1. MPSoC applications offer lots of network-level concurrency
2. Packetization and serialization are the best way to minimize implementation costs
3. NoC latency is acceptable

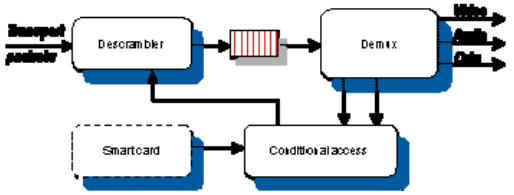
Concurrency in Consumer MPSoCs

Consumer MPSoCs process data in parallel, but communicate…

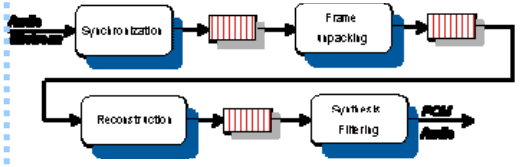




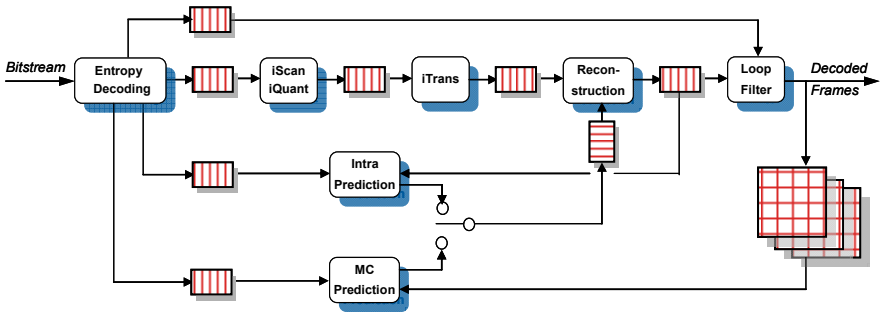
Transport demux



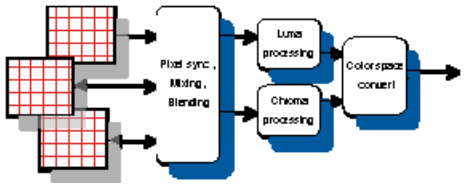
Audio Decode



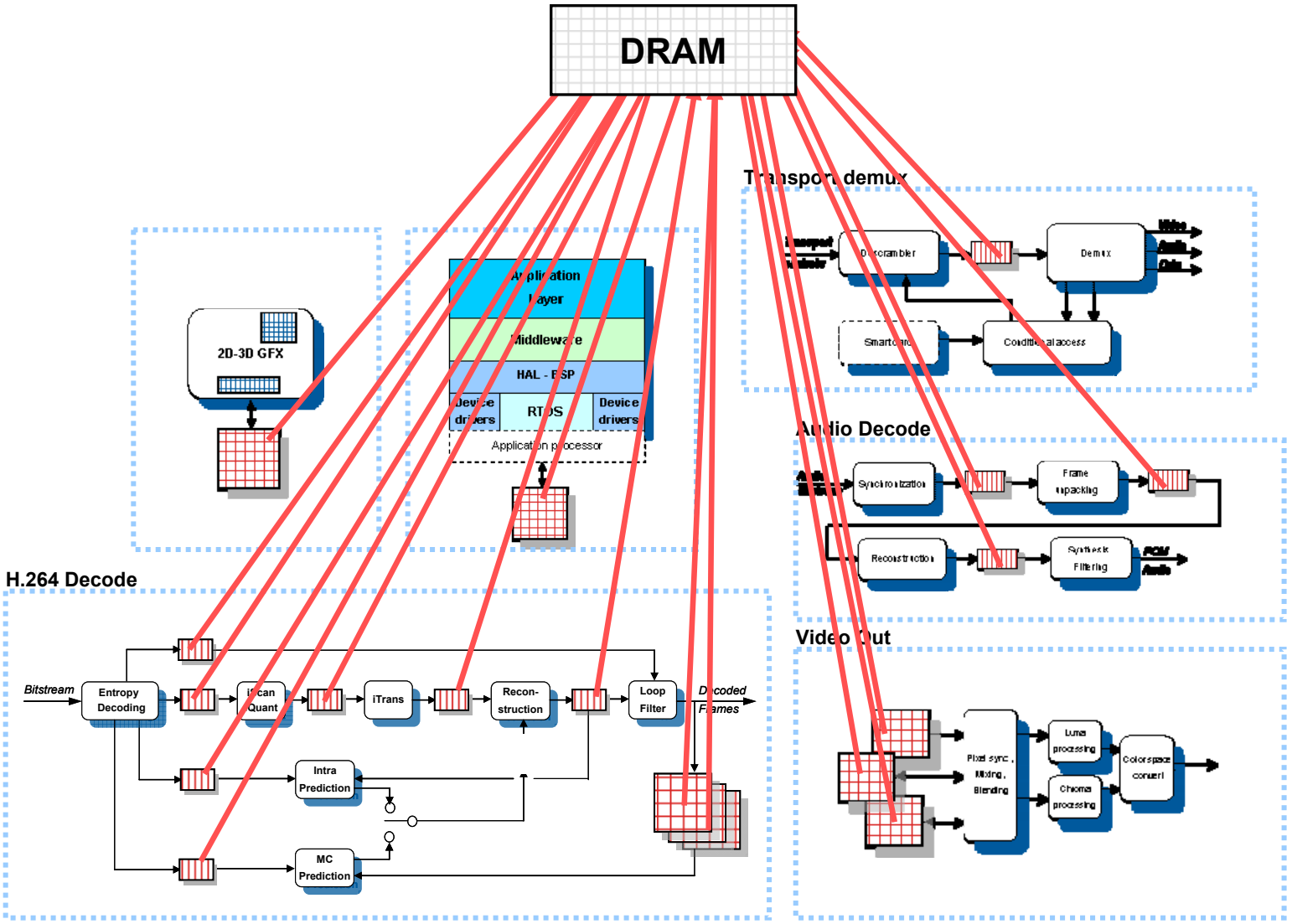
H.264 Decode



Video Out



Concurrency in Consumer MPSoCs



From MPSoC '07: High-perf. multithreaded memory subsystems for MPSOCs

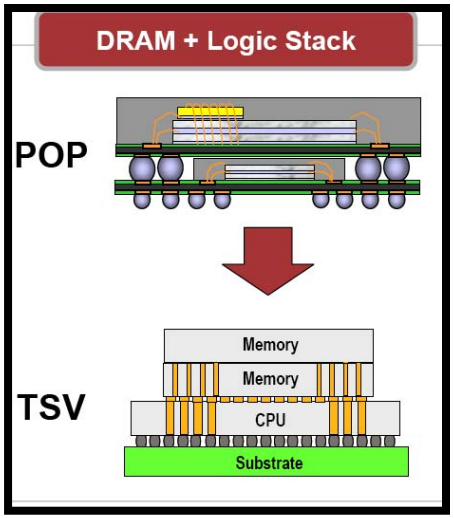
Single-port DRAM Subsystem Protocols

Ordering/ flow control	In-order/ blocking	Out-of-order/ blocking	Out-of-order/ non-blocking
Peak BW limited by	DRAM	DRAM	DRAM
Ordering flexibility	None	High	High
Queuing	None	Shared	Per-thread
Compiled RAM-friendly	No	No	Yes
Init. BW==DRAM BW	Yes	Yes	No
DRAM efficiency	Medium	High	High
Max. CPU latency	High	Medium	Low
Data interleaving	None	Minor	High

MPSoC DRAM Problems and Opportunities

- Problems in current systems
  - In consumer & mobile SoCs, DRAM ***bandwidth*** needs grow faster than ***capacity*** needs
  - Scaling DRAM bandwidth requires ***extra DRAMs***
    - And power-hungry PHYs
  - Wider DRAM interfaces & deeper pipelining increases access ***granularity***, driving need for ***multichannel*** aproaches
    - Which causes extra pin costs (after 2 channels)
  - Current DRAM interfaces are a ***bottleneck*** between
    - Lots of parallel initiators (data clients)
    - Lots of parallel DRAM banks (data servers)
- What if we could get rid of the interface bottleneck?
  - And be limited by DRAM bank bandwidths, instead
  - Without needing fancy PHYs

Wide I/O: TSV-enabled Mobile DRAM

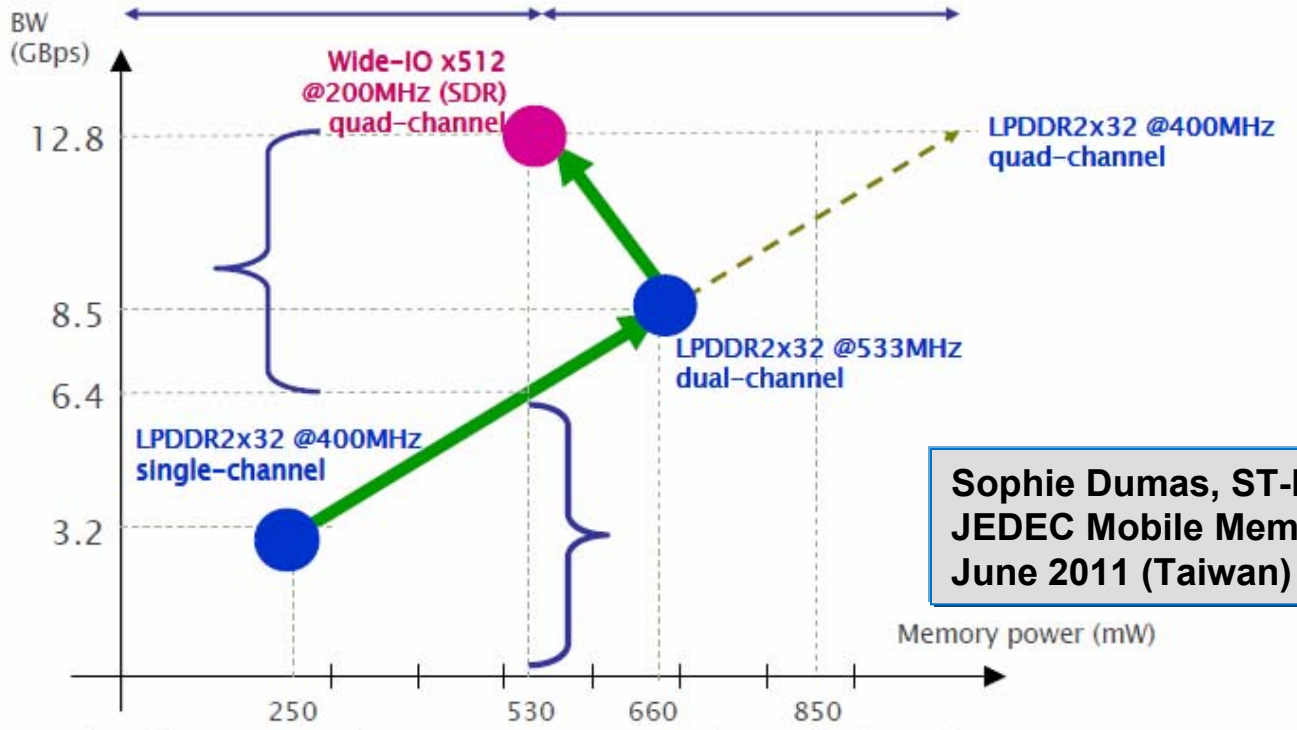


- Pending JEDEC standard (JC 42.6)
- High bandwidth, even at low capacity
  - Like 4 (x32) channels of LPDDR2-800
  - 12.8 GBytes/sec peak bandwidth
- Lowest power
  - No PHY (simple drivers/receivers, no PLL/DLL)
  - Low loading (capacitance and inductance)
  - Modest frequency (200 MHz)
- Smallest form factor
  - 3D stacked based on thin (50µm) TSV-based die
- Minimal change to DRAM design (ex-TSV)
- Risks are all TSV-related (cost, yield, biz model)
- Smartphone market will drive volumes

Wide I/O Power Estimates

WideIO Positioning

WideIO offers twice the BW of LPDDR2 for same power

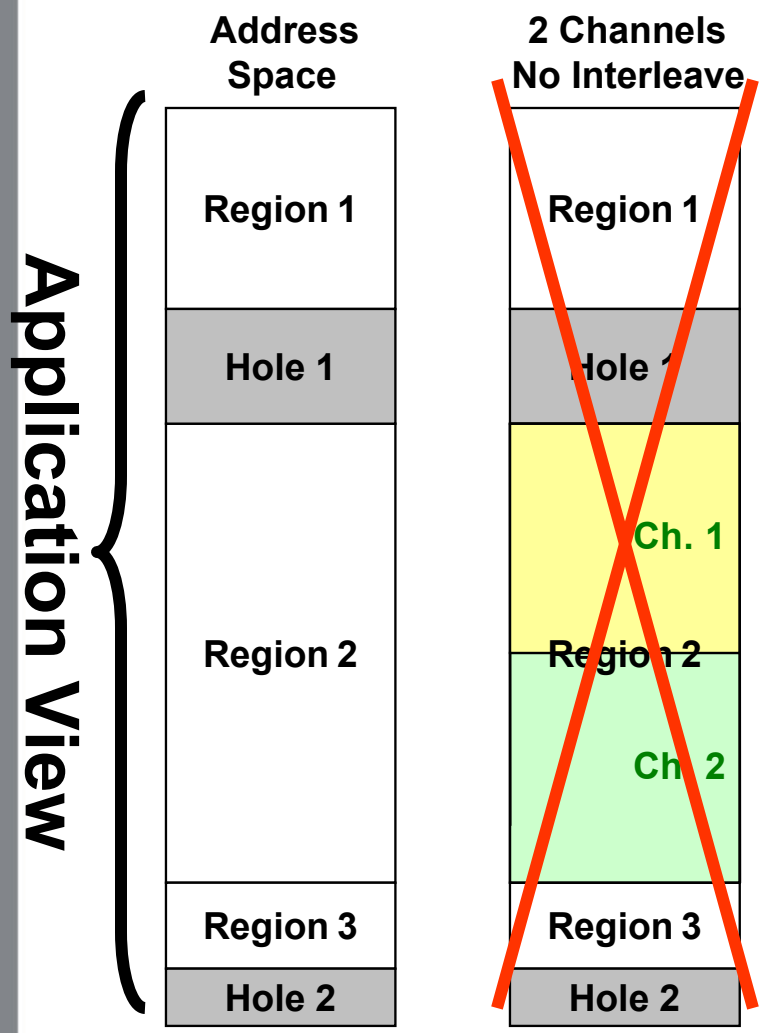


Note: IDD4 (Data toggle 50%), Memory controller + DRAM, LPDDR2 8pF, Wide IO 2pF (2-die stack)

JEDEC Global Standards for the Microelectronics Industry

Sophie Dumas, ST-E
JEDEC Mobile Memory Forum
June 2011 (Taiwan)

Multichannel DRAM System Challenges



Key Problems:

- Load balancing
  - Must balance memory traffic evenly among channels
- Maintaining throughput
  - Multiple channels cause throughput & ordering issues for pipelined memories

Software and IP cores must manage multiple channels explicitly

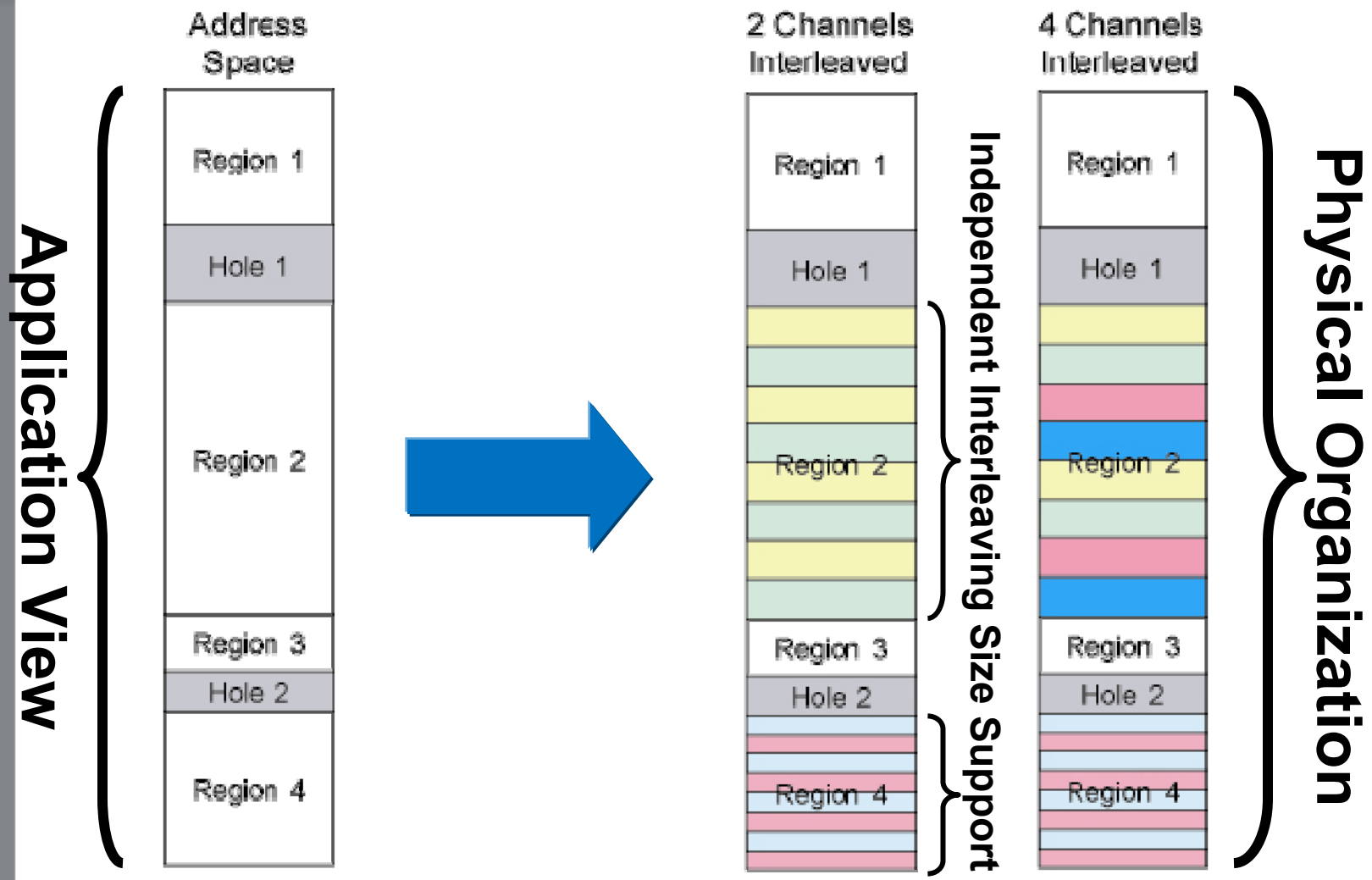
Interleaved Multichannel Technology (IMT*): Seamless Transition to Multichannel

*patents pending

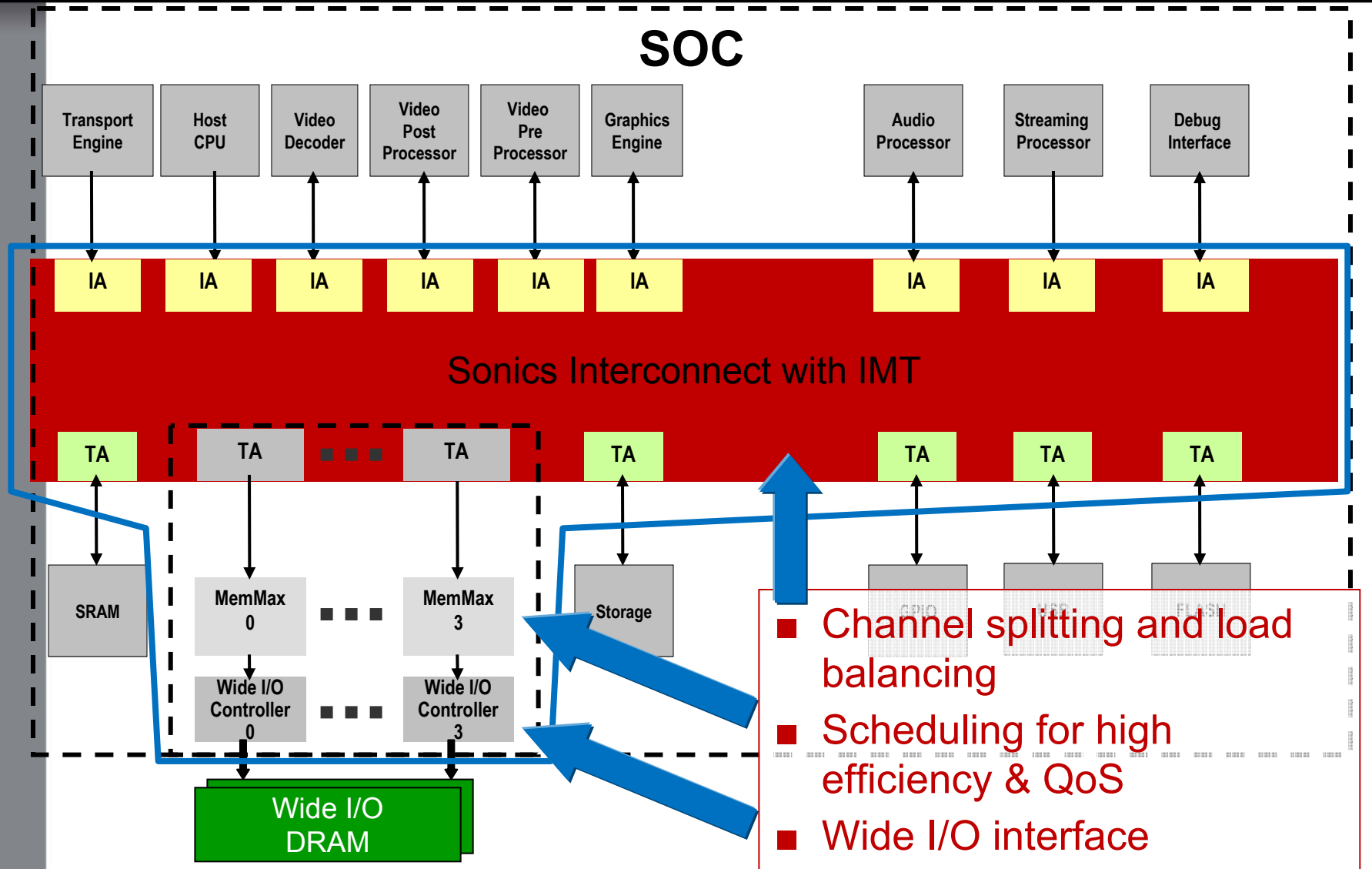
- Interleaving support requires splitting (and chopping!) traffic for delivery to proper channel
  - Splitting in memory controller *creates performance and routing congestion bottleneck*
- Predictably high performance
  - *Automatically spreads traffic* across channels to ensure load balancing
  - Keeps DRAMs operating at full throughput *without costly reorder buffers*
- Scalable architecture
  - Up to 8 interleaved channels within the same address region
  - *Fully distributed* to avoid bottlenecks & placement restrictions
- Application flexibility
  - *Transparent to software and initiator hardware*
  - Supports full or partial memory configurations – at run time

Multichannel Interleaving in the Interconnect
Higher Performance, Lower Area, More Scalable

IMT: Transparent to System, Optimized for Performance



Complete Wide I/O System Solution



- Channel splitting and load balancing
- Scheduling for high efficiency & QoS
- Wide I/O interface

Summary

- Consumer MPSoCs performance still dominated by DRAM
- Bandwidth requirements driving multichannel approaches
  - Increasing target-level parallelism for networks
- New JEDEC Wide I/O standard offers compelling performance and power benefits
  - Assuming TSV-related issues can be managed
- MPSoC solutions with transparent load balancing unlock the potential of 3D multichannel DRAMs
  - If they maintain high DRAM efficiency and QoS