ADVANCE PROGRAM

SUNDAY JULY 14: WELCOME

18:00 **Registration**

19:00 **Welcome reception**

MONDAY JULY 15

9:00 **Registration continued**

SESSION 1: KEYNOTE

9:00 **Chinhyun (Thomas) Kim, Samsung Electronics Ltd., Korea**
Challenges of Mobile Application Processor Development

10:00 **Break**

SESSION 2: DATA CENTER AND ADAPTIVE COMPUTING

10:30 **Giovanni Beltrame, École Polytechnique de Montréal, Canada**
Self-Adaptive Computing for Many-Core Processors

11:00 **Rui Hou, Chinese Academy of Sciences, China**
Cost-effective Data Center Server

11:30 **John Goodacre, ARM, UK**
Scaling Mobile Compute to the Data Centre

11:42 **Panel with the lecturers (for Sessions 1 and 2)**

12:30 **Lunch**

SESSION 3: MANYCORE

14:00 **Masaaki Kondo, The University of Electro-Communications, Japan**
SMYLEref: A Reference Architecture for Manycore-Processor SoCs

14:30 **Masaki Gondo, eSOL Co.,Ltd., Japan**
A Many-Core realtime OS (MCOS)

15:00 **Emil Matus, Technical University Dresden, Germany**
Challenges for Resource Management in Communications Manycore Architectures

15:12 **Break**

SESSION 4: MULTIMEDIA

15:45 **Mei Chen, Intel, USA**
Architecture and algorithms for reactive multi-modal sensing, illumination, and displays

16:15 **Takashi Miyamori, Toshiba Corporation, Japan**
Image Sensing and Processing: A New Challenge of MPSoCs

16:27 **Masaitsu Nakajima, Panasonic, Japan**
Multicore SoC for 4k2k Era

16:39 **Pieter van der Wolf, Synopsys, Netherlands**
Scalable Multicore Audio Solutions

16:51 **Panel with the lecturers (for Sessions 3 and 4)**

TUESDAY JULY 16

SESSION 5: KEYNOTE

9:00 **Hiroshi Nakamura, The University of Tokyo, Japan**
Challenges and Opportunities of Normally-Off Computing

10:00 **Break**

SESSION 6: SMART SENSOR

10:30 **Tohru Shimizu, Renesas Electronics Corporation, Japan**
Normally-off Computing and its Application to the Sensor-Net

11:00 **Yankin Tanurhan, Synopsys, USA**
Smart Sensor Systems The Next Multiprocessor Challenge

11:30 **Koichiro Yamashita, Fujitsu Laboratories Ltd., Japan**
A principle simulator for architecture design of distributed multi-node sensor system

11:42 **Panel with the lecturers (for Sections 5 and 6)**

12:30 **Lunch**

SESSION 7: HIGH-PERFORMANCE ACCELERATION

14:00 **Soojung Ryu, Samsung Advanced Institute of Technology, Korea**
Multi-SRP Architecture for High Performance Computing

14:30 **Michel Laurence, École de technologie supérieure (ETS) /Octasic Inc., Canada**
Low-Power High-Performance Asynchronous General Purpose ARMv7 for Multi-Core Applications

15:00 **Akira Asato, Fujitsu, Japan**
Accelerating Scientific Applications on Fujitsu's Supercomputer

15:12 **Kiyoung Choi, Seoul National University, Korea**
Mapping Control Flows onto CGRA

15:24 **Koji Inoue, Kyushu University, Japan**
Accelerating Predictive Model Control Applications on Manycores

15:36 **Break**

SESSION 8: KEYNOTE

16:00 **Manju Hegde, AMD, USA**
Heterogeneous System Architecture (HSA) and its implications for the software ecosystem

SESSION 9: EMERGING MEMORY AND INTERCONNECT

17:00 **Yuan Xie, Penn State/AMD Research, USA**
Improving Non-Volatile Cache Lifetime by Reducing Inter- and Intra-Set Write Variations

17:12 **Sungjoo Yoo, POSTECH, Korea**
Addressing Resistance Drift Problem in Multi-Level Cell Phase-Change RAM

17:24 **Panel with the lecturers (for Sessions 7, 8, and 9)**

WEDNESDAY JULY 17

SESSION 10: KEYNOTE

9:00 **Hiroto Yasuura, Kyushu University, Japan**
Dependability Issues on MPSoC

10:00 **Break**

SESSION 11: HARDWARE TECHNIQUE

10:30 **Youn-Long Lin, National Tsing Hua University, Taiwan**
Intra-Frame Video Compression for Bus Traffic and Memory Reduction

10:42 **Chris Rowen, Cadence, USA**
Grand Challenge Scaling - Pushing a Fully Programmable TeraOp into Handset Imaging

10:54 **Shinobu Fujita, Toshiba, Japan**
Progress of STT-MRAM and its Challenge towards Normally-off-Multi-core SoC

11:24 **Pierre G. Paulin, STMicroelectronics Inc., Canada**
OpenCL Programming Tools for the STHORM Multi-Processor Platform: Application to Computer Vision

11:36 **Panel with the lecturers (for Sessions 10 and 11)**

12:30 **Lunch**

SESSION 12: INTERCONNECTION NETWORK / ARCHITECTURE

14:00 Joël Monnier, Kalray, France
Manycore Challenges for the Next Generation of Professional Applications

14:30 Jiang Xu, Hong Kong University of Science and Technology, Hong Kong
Inter/Intra-Chip Optical Networks: Opportunities and Challenges

15:00 Yuichi Nakamura, NEC Corp., Japan
How to Use Commercial Many Core Systems for Multimedia Applications

15:12 Marcello Coppola, STMicroelectronics, France
Virtualization-ready SoC: Challenges for Heterogeneous Multi-core Architectures

15:24 Gabriela Nicolescu, Ecole Polytechnique de Montréal, Canada
Transient Thermal Simulation for 3D ICs with Liquid Cooling and Through Silicon Vias

15:36 Kees Vissers, Xilinx, USA
Programming vision applications on Zynq using OpenCV and High-Level Synthesis

15:48 Kees van Berkel, STEricsson, Eindhoven University of Technology, France
Processor Versatility, an attempt at definition and quantification

16:00 Panel with the lecturers (for Session 12)

16:45 Speaker's Meeting

THURSDAY JULY 18

SESSION 13: KEYNOTE

9:00 Shorin Kyo, Renesas Electronics Corporation, Japan
Multi/many-core Processing Prospective for Embedded Computer Vision

10:00 Break

SESSION 14: VIRTUALIZATION / DESIGN METHODOLOGY

10:30 Rainer Leupers, RWTH Aachen University, Germany
Two new Use Cases for Virtual Platforms

10:42 Raphaël David, CEA LIST, France
Multi-criteria exploration framework for MPSOC

10:54 Samar Abdi, Concordia University, Canada
Hybrid Prototyping of MPSoCs

11:06 Gerd Ascheid, RWTH Aachen University, Germany
Processing energy vs. performance: Conclusion from a multi-core design

11:18 Norbert Wehn, University of Kaiserslautern, Germany
Multi-Gigabit Channel Decoders

11:30 Panel with the lecturers (for Sessions 13 and 14)

12:30 Lunch

SESSION 15: SIMULATION

14:00 Ghislain Kaiser, Docea Power, France
Coupled power/thermal simulation to optimize the operating point of complex multi-core SoCs

14:30 Hiroyuki Tomiyama, Ritsumeikan University, Japan
Simulation of Many-core NoCs with QEMU and SystemC

14:42 Tsuyoshi Isshiki, Tokyo Institute of Technology, Japan
Trace-Driven MPSoC Simulation with Cache Modeling

14:54 Frédéric Pétrot, TIMA Lab, Grenoble University, France
Using Hardware-Assisted Virtualization for Native Simulation of MPSoC

15:06 Break

SESSION 16: LOW POWER / ENERGY HARVESTING

15:40 Jenq-Kuen Lee, National Tsing-Hua University, Taiwan
Compiler for Low-Power with Parallel Design Patterns on Embedded Multi-Core Systems

16:10 Hironori Kasahara, Waseda University, Japan
OSCAR Parallelizing Compiler and Its Performance for Embedded Applications

16:22 Keiji Kimura, Waseda University, Japan
OSCAR API v2.1 with Flexible Accelerator Control Facilities

16:34 Tohru Ishihara, Kyoto University, Japan
Power Management Techniques for Energy Harvesting Embedded Systems

16:46 Edith Beigne, LETI, France
A fully energy-driven Power Management Unit in the scope of future energy harvesting complex systems

16:58 Yoshinori Takeuchi, Osaka University, Japan
Task Allocation and Scheduling for Voltage Frequency Island based MPSoC

17:10 Panel with the lecturers (for Sessions 15 and 16)

FRIDAY JULY 19

SESSION 17: KEYNOTE

9:00 Babak Falsafi, EPFL, Switzerland
Big Data and Dark Silicon: Taming Two IT Inflection Points on a Collision Course

10:00 Break

SESSION 18: GRAPHICS / VIDEO PROCESSING

10:30 Xiaoyao Liang, Shanghai Jiao Tong University, China
An Energy-Efficient and Scalable eDRAM-Based Register File Architecture for GPGPU

11:00 Eisaku Ohbuchi, Digital Media Professionals Inc., Japan
Low power graphics/computing architecture for embedded systems

11:30 Yukoh Matsumoto, TOPS Systems Corporation, Japan
SMYLEvideo distributed stream processing Heterogeneous Manycore architecture for Video Mining Applications

11:42 Panel with the lecturers (for Sessions 17 and 18)

12:30 Lunch

More information: http://www.mpsoc-forum.org/