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MPSoC'13
July 15-19, 2013
Otsu, Japan

Multi-Gigabit Channel Decoders

"Ten Years After"

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DFG Deutsche Forschungsgemeinschaft

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Multi-Megabit Channel Decoder

MPSoC'03
N. Wehn

UMTS standard: **2 Mbit/s** throughput requirements

NoC based Multi-ASIP Turbo-Code Decoder

- Heterogeneous communication network: busses and ring NoC
- Optimized Tensilica cores for MAP decoding
- Synthesis-based, 0.18um technology, UMTS compliant (K=5114, 5 iterations)

Total Nodes (N)	# of Clusters (C)	Cluster Nodes (N_C)	Throughp.* [Mbit/s]	Area Comm. [mm^2]	Area Total [mm^2]	Efficiency [Mb/s*mm^2]
1	1	1	1.48	NA	6.42	1
5	1	5	7.28	0.21	14.45	2.19
6	2	3	8.72	0.66	16.73	2.26
8	4	2	11.58	1.25	20.91	2.40
12	6	2	17.18	2.02	28.92	2.58
16	8	2	22.64	2.88	36.98	2.66
32	16	2	43.25	7.29	70.26	2.67
40	20	2	52.83	10.05	87.47	2.62

* Validated with Tensilica Xtensa API Interface, Tensilica ISS simulator

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Multi-Megabit Channel Decoder

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Dedicated Implementation

- VHDL-Model of fully parameterizable scalable Turbo-Decoder
- Synthesis and Power-Characterization with Synopsys Design Compiler on a 0.18 µm Standard Cell Library
- Validated in UMTS environment
- 166 MHz Log-MAP Implementation with 6 Turbo Iterations

Parallel SMAP Units N_D	1	4	6	6	6	8	8
Parallel I/O N_{IO}	1	1	1	2	con. I/O	1	2
Total Area [mm^2]	3.9	9.2	13.3	13.0	18.0	15.9	17.3
Fraction of Memory	85%	69%	69%	68%	77%	61%	64%
Energy per Block [mJ]	48.7	51.7	55.2	50.9	55.2	57.6	55.2
Throughput [MBit/s]	11.7	39.0	50.6	59.6	72.6	59.7	72.7
Efficiency (norm.)	1.00	1.32	1.12	1.47	1.19	1.05	1.24

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Multi-Gigabit Requirements

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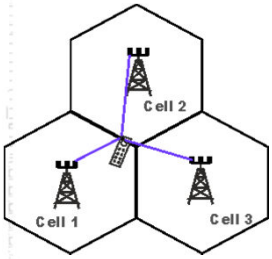
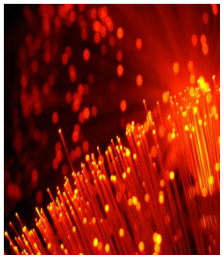
- Mobile traffic increases 60%/year until 2017
- New Communication Standards e.g. LTE-Advanced
- New techniques e.g. Coordinated Multipoint (CoMP), multi-user MIMO





- CoMP: 4 users/sector with 75 Mbit/s each
- Three sectors and 1 CoMP iteration: 4 x 75 x 3 x 2 = 1.8 Gbit/s
- IEEE 802.3an (10 GBASE T): 10Gbit/s
- IEEE 802.3ba standard: 100Gbit/s Ethernet speed
- Future: fiber channel 100Tb/s

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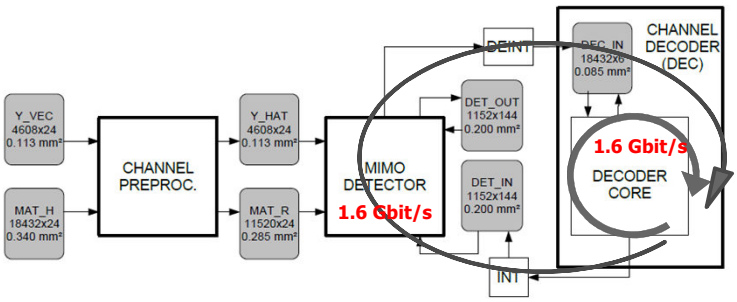
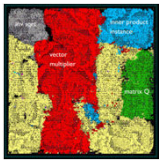
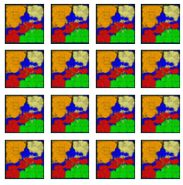
MIMO Receiver 4x4, 16 QAM



All designs in 65nm tech-nology, 200 MHz clock frequency



0.14 mm², 1 instance



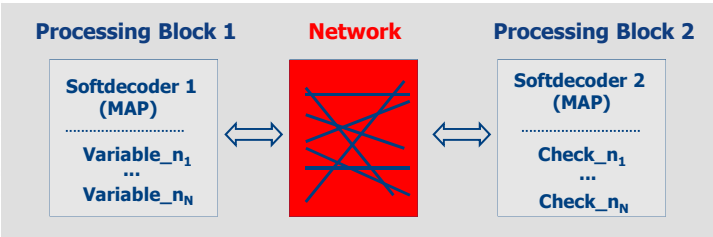
0.21mm²/instance
16 instances

4.6 mm², 1 instance

- System throughput **200 Mbit/s**
- 4 outer iterations, 5 decoder iterations: **1.6 Gbit/s** for detector & decoder
- Sphere decoder: 4 symbols ⇒ easy to parallelize, but decoder: 14880 bits

Generic Decoder Structure

- Most advanced channel codes: Turbo-Codes (HSPA, LTE), LDPC (DVB-S2)
- Iterative decoding algorithm performed on complete block with interleaved data exchange between processing blocks



Parallelize block processing

- Turbo-Code Decoder: **softdecoder inherent serial**
- LDPC Decoder: **inherent parallel** since node processing independent

Network (interleaver, tanner graph): **no locality**

- Routing congestion, access conflicts
- Impact on communication standards (UMTS/HSPA versus LTE)

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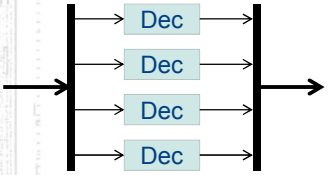
How to Increase Throughput?

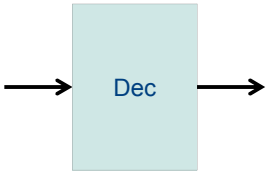
Use multiple slow decoders



PRO
- Easy to implement

CON
- Low efficiency, large memory
- Large latency

Use monolithic high speed decoder



PRO
- Higher efficiency
- Lower latency

CON
- Challenging architecture due to iterative decoding

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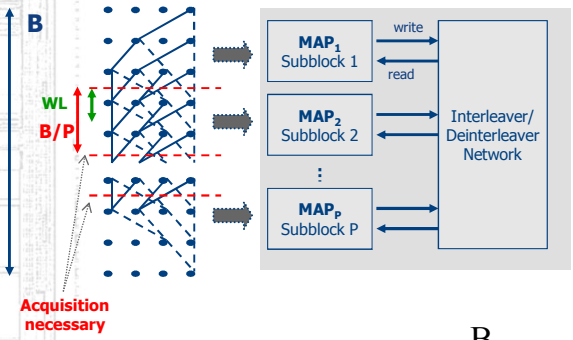
State-of-the-Art Turbo-Code Decoders

Softdecoder **inherent serial:** serial fwd/bwd recursion on complete block
⇒ challenge: parallelize MAP decoding



- **P** MAP decoder in parallel
- LTE conflict-free interleaver up to parallelism of 64
- Subblock size: **B/P**
- Windowing inside MAP to reduce memory (sliding window of size **WL**)

$$TP_{MAP} = \frac{B}{(B/P + L_{MAP}) * n_{half\_iter}} * f$$

$$L_{MAP} = L_{pipeline} + L_{WL} + L_{ACQ}$$

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Turbo-Code Decoder

$$TP_{MAP} = \frac{B}{(B/P + L_{MAP}) * n_{half\_iter}} * f; \quad L_{MAP} = L_{pipeline} + L_{WL} + L_{ACQ}$$

High Throughput (high code rates) ⇒ large P

- Communications performance decreases for high code rates with small L_{ACQ}
- Increase L_{ACQ} to counterbalance communications performance decrease

⇒ L_{MAP} dominates: saturation in throughput

- **Smaller P**: Radix 2 ⇒ Radix 4 only P/2 for same throughput
- **Smaller L_{ACQ}**: Next iteration initialization (NII) L_{ACQ} =0
- **Smaller L_{WL}**: no windowing inside MAP ⇒ L_{WL}=0
  - Improves communications performance
  - But second LLR unit mandatory and increase in memory
- **Re-computation:** only every n*th* metric is stored. Additional state metric unit re-calculates the other n-1 metrics. Optimum n=$\sqrt{B/2P}$

  E.g. LTE: reduces memory storage from B=6144 to 768 state metrics

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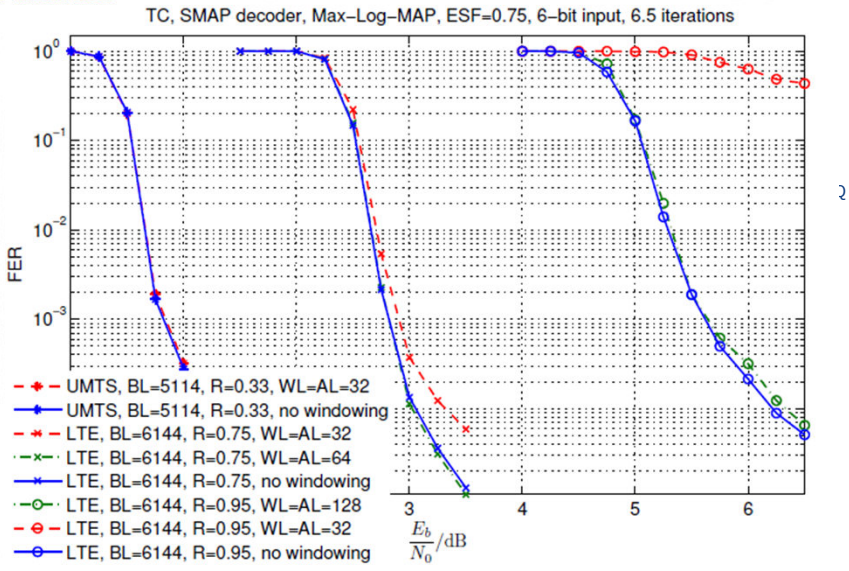
Turbo-Code Decoder



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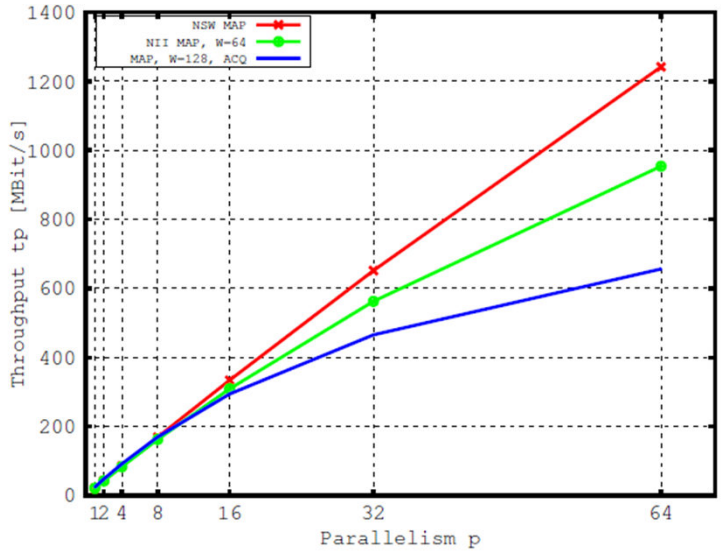
Throughput dependent on Parallelism



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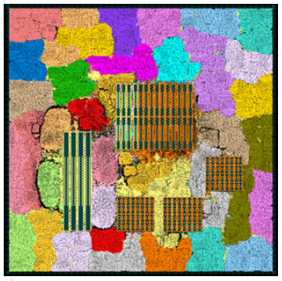
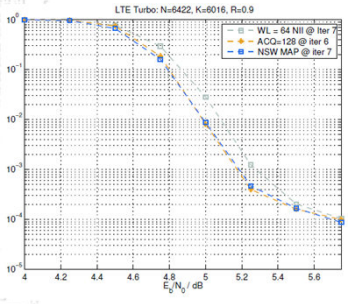
2.15 Gbit/s LTE TC Decoder@65nm





	This work	[13]	[14]	[15]
Radix and Parallelism	4/32	2/64	2/8	4/8
Throughput $[MBit/s]$ @Clock f $[MHz]$	2150 @ 450	1200 @ 400	150 @ 300	390 @ 302
Parameters affecting communications performance				
Iterations	6	6	6.5	5.5
Acquisition	NII	NII	96 + NII	30
Window length	192	64	32	30
Input quantization	6	6	6	5
Technology $[nm]$	65	65	65	130
Voltage	1.1V	0.9V	1.1V	1.2V
Area $[mm^2]$	7.7	8.3	2.1	3.57
Area Efficiency @6 Iter $[MBit/s/mm^2]$	279	145	77	Not fair, 130nm

[13] Y. Sun and J. Cavallaro, "Efficient hardware implementation of a highly-parallel 3GPP LTE/LTE-advance turbo decoder," *Integration VLSI Journal*, 2010.

[14] M. May, T. Ilnseher, N. Wehn, and W. Raab, "A 150Mbit/s 3GPP LTE Turbo Code Decoder," in *Proc. Design, Automation and Test in Europe, 2010 (DATE '10)*, Mar. 2010, pp. 1420–1425.

[15] C. Studer, C. Benkeser, S. Belfanti, and Q. Huang, "Design and Implementation of a Parallel Turbo-Decoder ASIC for 3GPP-LTE," *IEEE Journal of Solid-state Circuits*, vol. 46, no. 1, pp. 8–17, Jan. 2011.

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Multi-Gigabit Decoder

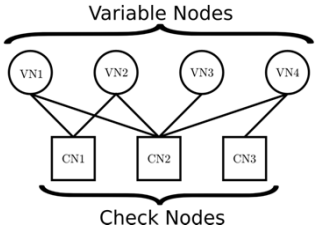
MAP Parallelism >64

- Architecture efficiency largely decreases
- Use multiple instances of a decoder
- What about unrolling the iterative loop?

LDPC Decoder

- Inherent parallel
- Defined via sparse parity check matrix H

$$H = \begin{pmatrix} 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{pmatrix}$$



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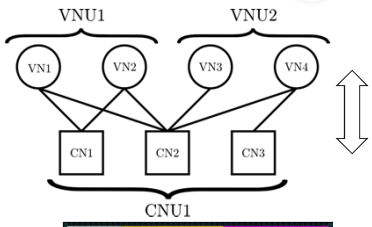
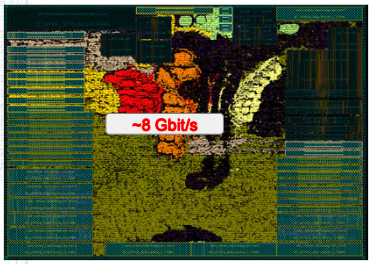
Multi-Gigabit LDPC Decoder

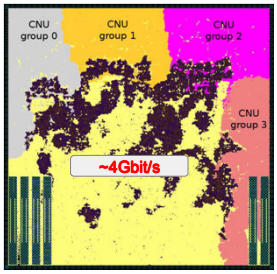
Partially parallel LDPC decoder

- Large block sizes e.g. DVB S2 64800
- Limited throughput
- But large flexibility e.g. code rates





UMIC LDPC Decoder
Codeword length: 3720-14880
Parallelism: 279
7.5 Gbit/s, 5 iterations
65 nm technology, 4.6mm^2



LDPC Decoder IEEE 802.15.3c
Codeword length: 672
Parallelism: 336, 9 iterations
65nm technology, 1.15mm^2

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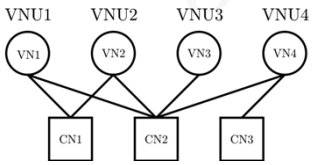
Multi-Gigabit LDPC Decoder

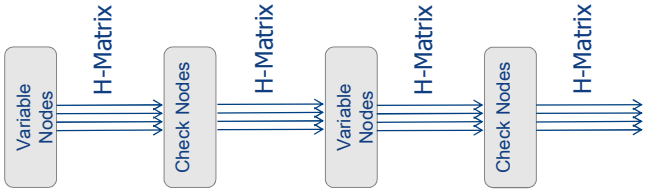


Full parallel architecture

- High throughput, e.g. 10 GBASE-T standard
- Smaller block sizes, limited flexibility
- Two-phase scheduling
- Routing congestion problems (>50% area)
- Throughput limited by iterative data exchange and routing congestion

Very high throughput

- Unrolling the iteration and pipelining
- Largely reduced routing complexity



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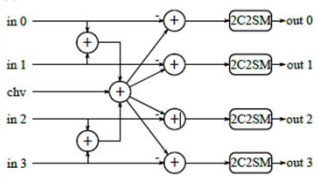
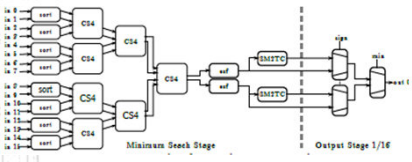
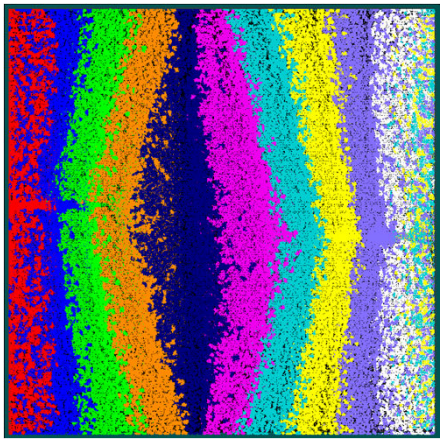
Multi-Gigabit LDPC Decoder

Fully parallel node architectures







IEEE 802.ad standard (WiGig)
Codword length: 672bit
9 iterations, 30 clock cycles latency
65nm technology

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Multi-Gigabit LDPC Decoder

Decoder	[14]	[15]	[16]	[17]	Proposed
CMOS Technology	65nm	65nm LVT	65nm	65nm	65nm SVT
Supply Voltage [V]	-	1.2	0.9	1.3	1.2
Frequency [MHz]	235	400	400	195	257
Standard	IEEE 802.15.3c	IEEE 802.15.3c	IEEE 802.3an	IEEE 802.3an	IEEE 802.11ad
Code Rate	7/8	1/2, 5/8, 3/4, 7/8	1723/2048	1723/2048	13/16
Level of Parallelism	partially parallel	partially parallel	partially parallel	fully parallel	fully parallel, unrolled
Scheduling	layered	layered	two-phase	two-phase	two-phase
Algorithm	min-sum	min-sum	min-sum	threshold min-sum	min-sum
Iterations	5	10	8	11	9
Quantization	6	6	4	5	4
Area [mm^2]	0.79	1.30	5.05	4.84	12.09
Throughput [Gbit/s]	7.9	6.7	8.5	36.3	160.8
Power Eff. [pJ/bit/Iter.]	-	8	11.76	3.36	3.61
Area Eff. [Gbit/s/mm^2]	10.0	5.2	1.7	7.5	13.6

[14] H. Shiran-Mehr, T. Mohsenin, and B. Baas, "A reduced routing network architecture for partial parallel LDPC decoders," in *Signals, Systems and Computers (ASILOMAR), 2011 Conference Record of the Forty Fifth Asilomar Conference on*, 2011, pp. 2192–2196.

[15] Z. Chen, X. Peng, X. Zhao, Q. Xie, L. Okamura, D. Zhou, and S. Goto, "A macro-layer level fully parallel layered LDPC decoder SOC for IEEE 802.15.3c application," in *VLSI Design, Automation and Test (VLSI-DAT), 2011 International Symposium on*, 2011, pp. 1–4.

[16] Z. Zhang, V. Anantharam, M. Wainwright, and B. Nikolic, "An Efficient 10GBASE-T Ethernet LDPC Decoder Design With Low Error Floors," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 4, pp. 843–855, 2010.

[17] T. Mohsenin, D. Truong, and B. Baas, "A Low-Complexity Message-Passing Algorithm for Reduced Routing Congestion in LDPC Decoders," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 5, pp. 1048–1061, 2010.

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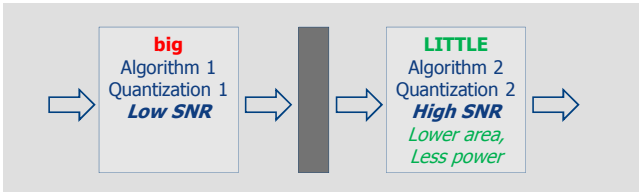
Multi-Gigabit Decoder

Exploit iterative behavior

- Different quantization for different iteration stages
- Different algorithms e.g. 3-min versus min-sum for different stages

big.LITTLE Approach

- "Partial unrolling"
- Optimized stages for different iteration groups & SNR



Energy optimization (dark silicon)

- Near subthreshold voltage: extreme parallelism necessary
- 10Gbit/s@20MHz: 1.2V ⇒ 0.5V yields ~ 3-5x improvement in energy efficiency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