# Normally-Off Computing for Smart City Applications

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# What is Normally-Off Computing?

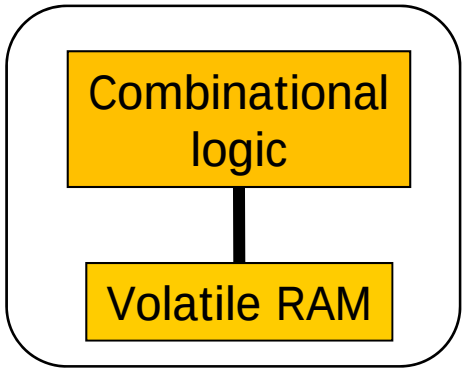
- Normally-Off (N-Off): aggressively powers off components of computer systems when they need not to operate, even under computation.
- Computing which realizes the 'Normally-Off'
- Key Technology
  - Non-Volatile Memory (MRAM, FeRAM, etc.)
  - Intelligent Power Management
- Strategy:
  - not a simple combination of these technologies
  - Computing which exploits synergy of these technologies

# Introduction of Normally Off Computing Project

- Project supported by NEDO/METI
  - Period : Sep. 2011 – Feb. 2016
  - NEDO : New Energy and Industrial Technology Development Organization
  - METI : Ministry of Economy, Trade and Industry
  - Participating Industries: Renesas, Toshiba, Rohm
  - Budget : Half-supported by Government
    (Approx.) $7M USD / year by NEDO + $7M USD / year by Industry
  - Project Leader : Hiroshi Nakamura (U. Tokyo)
- Update from MPSoC'13
  - Passed intermediate evaluation last year
  - Progress towards Practical Application

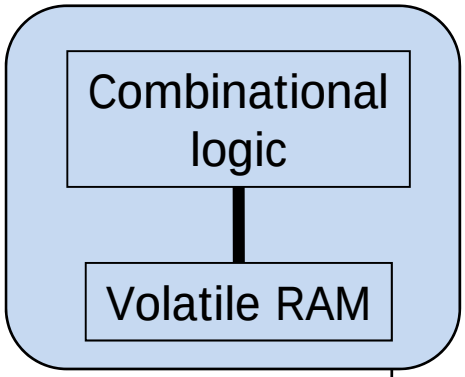
# Goal of Normally-Off Computing

So Far:




Always ON

Coarse-grained power gating



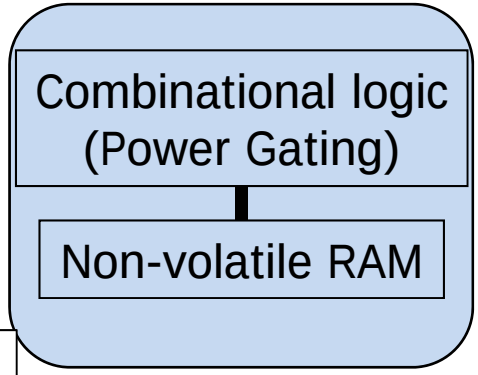

long time for data save

Non-volatile Storage

Power-off area

Power off as much as possible

Temporally and spatially fine-grained power gating

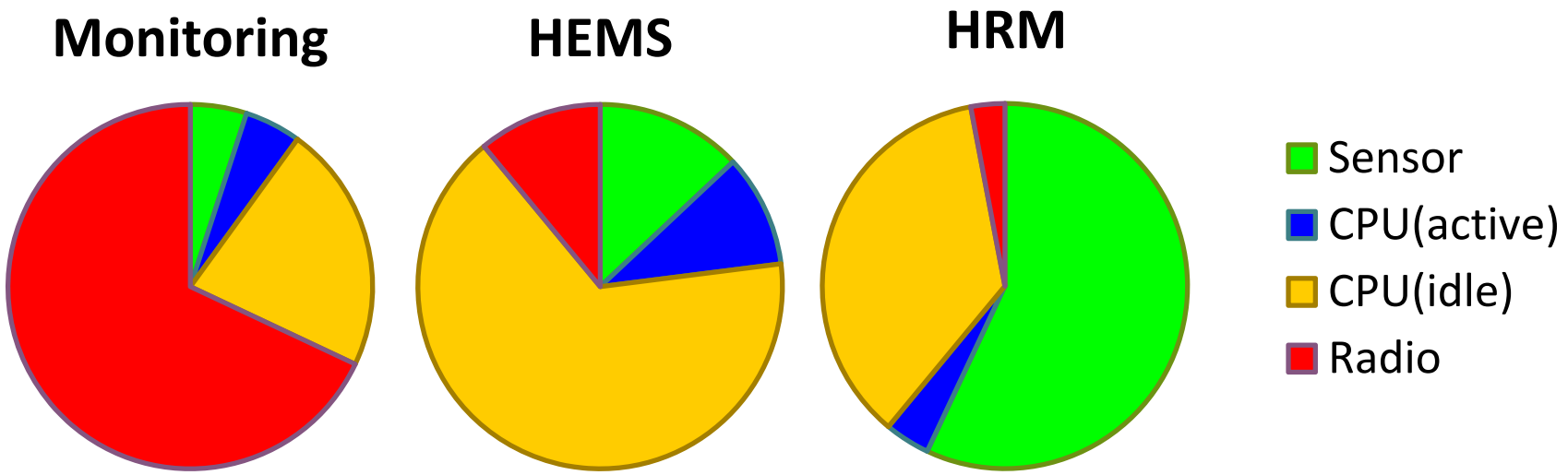



Characteristics of NV-RAM

- Zero Stand-by Power ☺
- Slow speed ☹
- Higher write Power ☹

Ideal Normally-Off

# Importance of Normally-Off: Power Breakdown of Sensor Node




- Wide Variety: depends on applications
- CPU(idle) is dominant
- Reduction of CPU Idle Power is important
  - Environment Monitoring (*)
  - HEMS (Home Energy Management System) [Courtesy of Hayashikoshi@Renesas]
  - HRM (Heart Rate Monitoring) (**)

(*) O. Landsiedel et al., "Accurate Prediction of Power Consumption in Sensor Networks," IEEE Workshop on Embedded Sensor Networks, 2005, pp.37-44
(**) S. Izumi et al., "A 14 µA ECG processor with robust heart rate monitor for a wearable healthcare system," IEEE ESSCIRC, 2013, pp. 145-148

# Challenges of N-Off Computing

- Temporal Granularity
  - Finer Granularity is preferable for Power Reduction

  BUT,

  - Too frequent power gating increases power consumption
  - Too frequent NV-RAM accesses consume larger power consumption

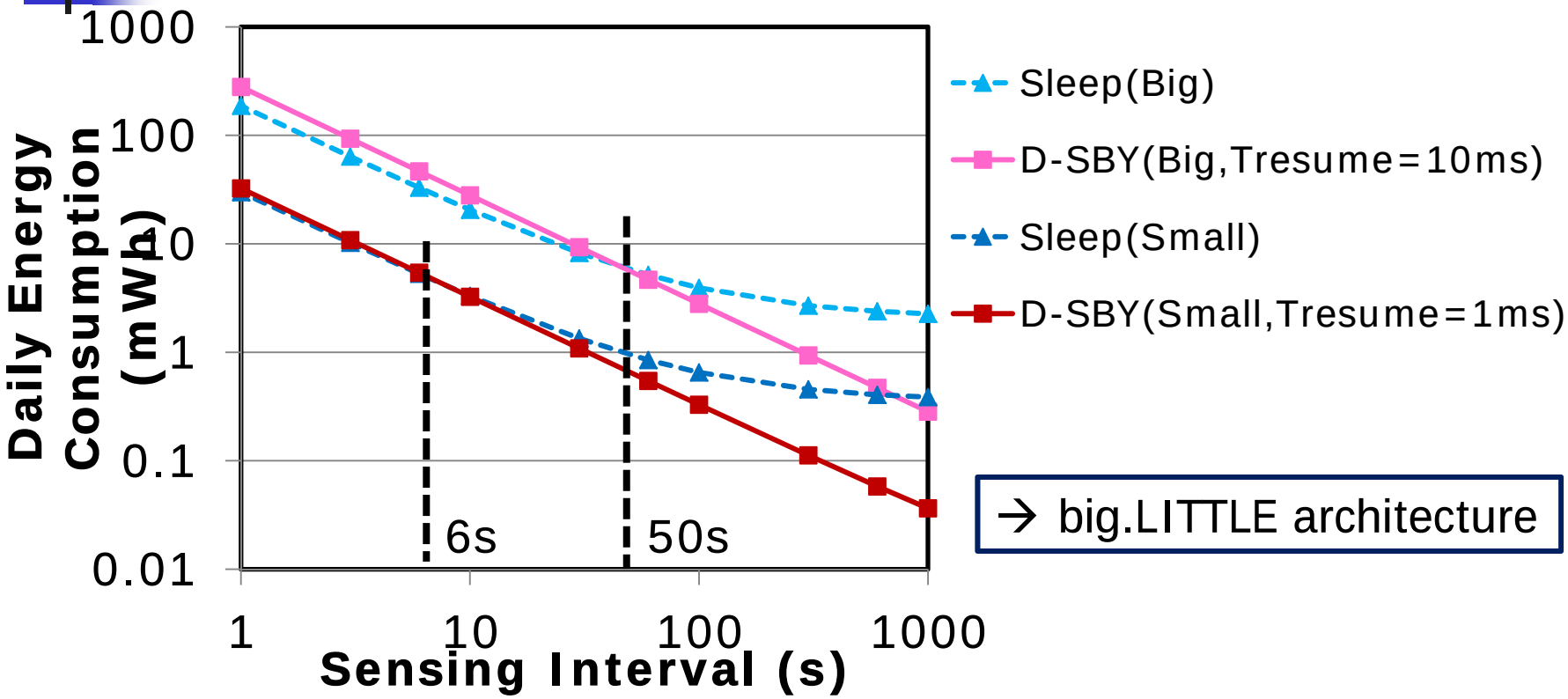
# Granularity of Power Management

- Available Low Power Mode:

  Sleep vs. Deep Stand-by (D-SBY)

  - Sleep : Clock Gating, Power Supplied
    - Quick Resume ☺, Small Energy for Resume ☺
    - Waste of Idle Power ☹
  - Deep Stand-by : Clock & Power gating
    - Slow Resume ☹, Large Energy for Resume ☹
    - Effective Suppression of Idle Power ☺
- Superiority depends on
  - Both System and Application Characteristics

# Sleep vs. Deep Stand-By

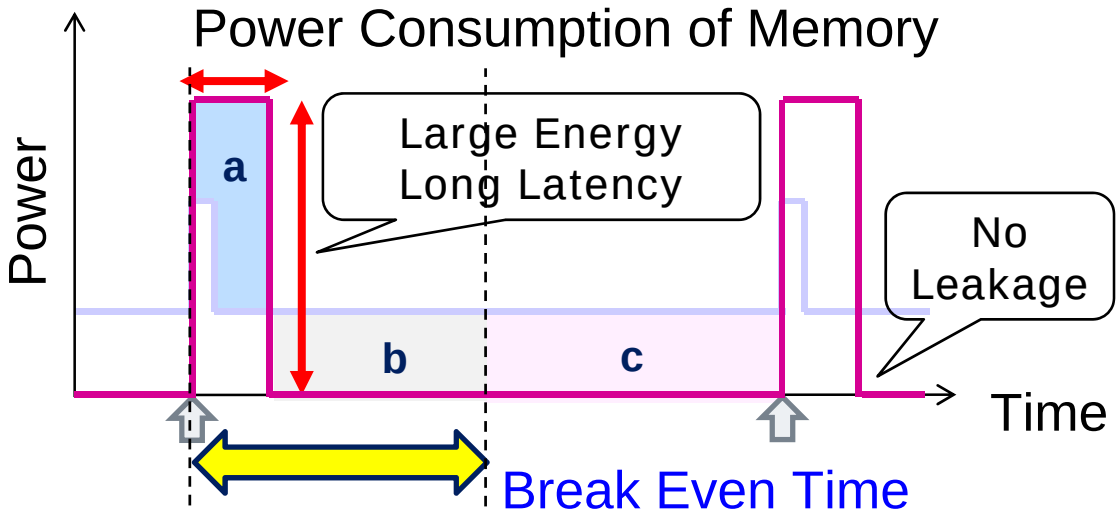



- Parameters Big Core, Little Core, Sensor & Radio

# Pitfall

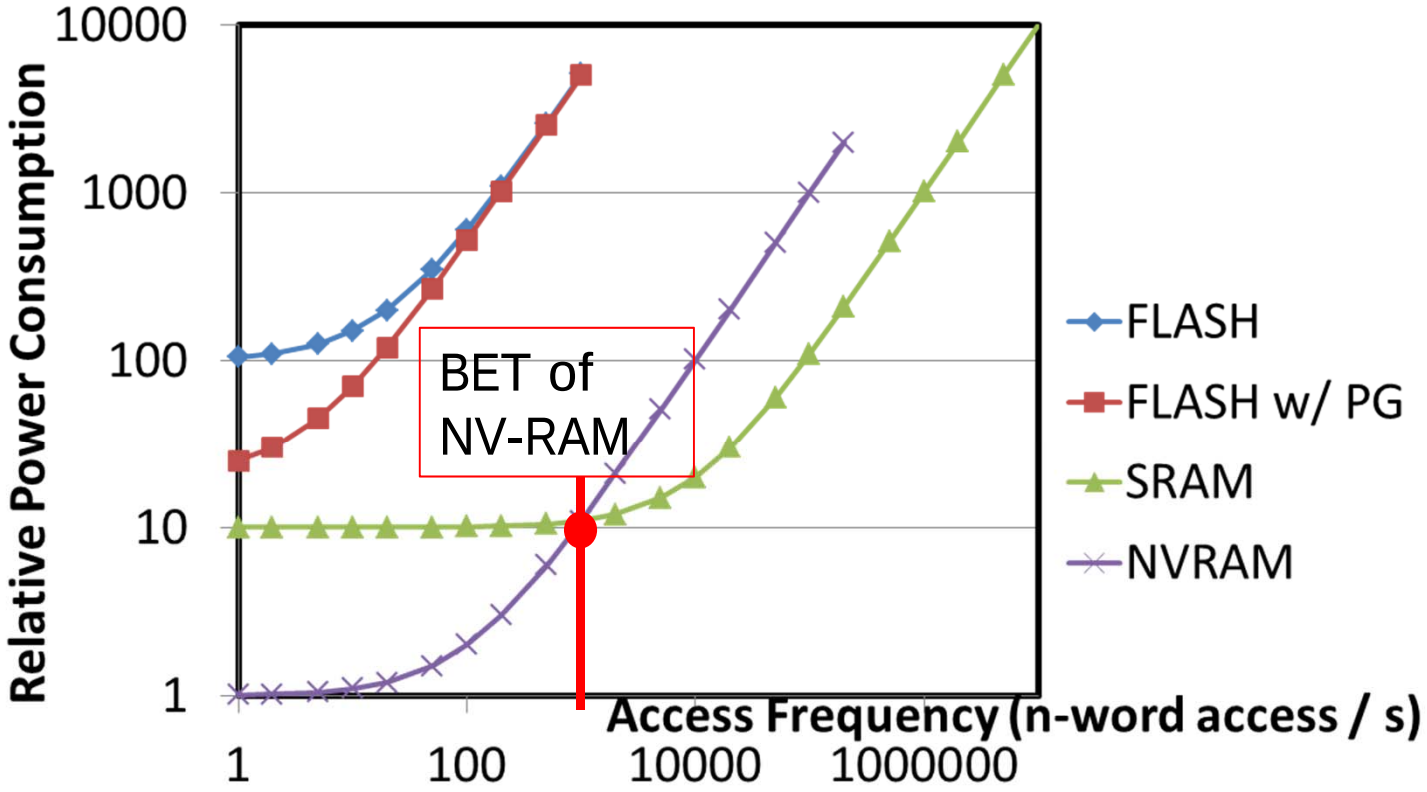
- Replacing volatile RAM with NV-RAM always leads to power reduction ← *This is FALSE*
- (Important) Access energy
  Non-volatile RAM ＞ Volatile RAM

→ Break Even Time of NV-RAM is important



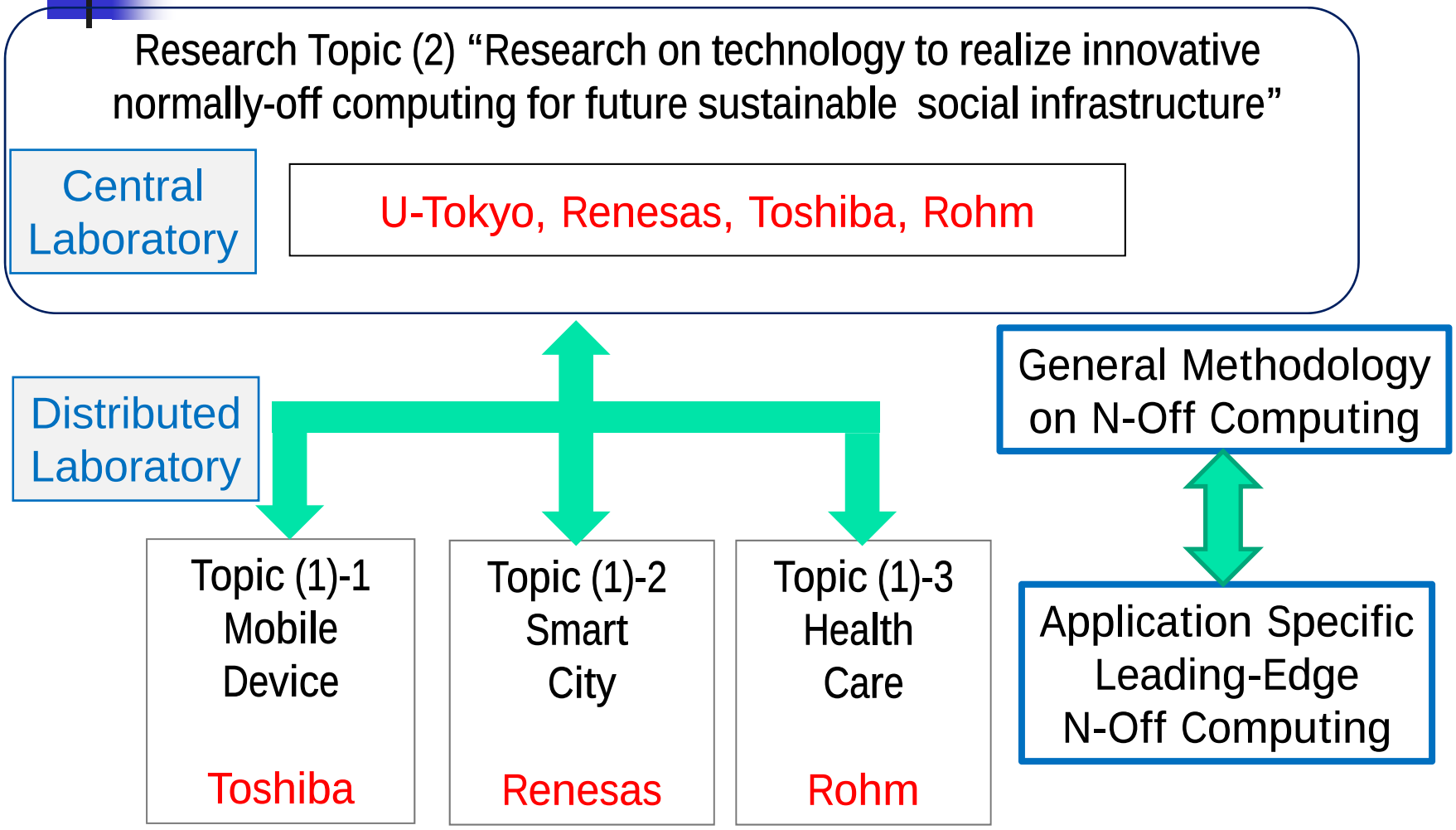

a : extra access energy
b : reduced leakage energy
c : actual reduced energy
Break Even Time (BET)
Time when “a” = “b”

# BET of Non-Volatile Memory




- BET of NV-RAM is 1sec when 1K words are written
- NV-RAM of low access power (=shorter BET) is preferable

# NEDO Project Organization



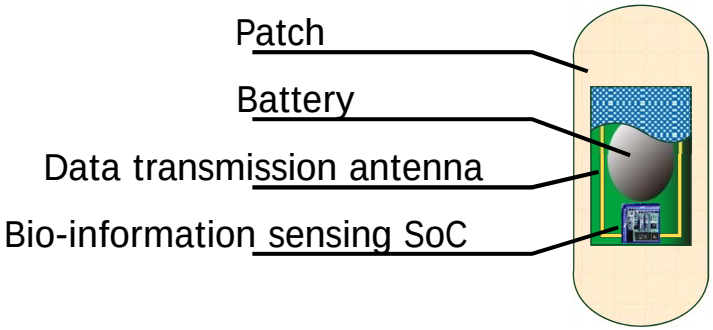
# Health Care (ROHM)

## ROHM + OMRON HEALTHCARE + Kobe Univ.

● 1st gen. Bio-information sensor

| | |
|---|---|
| Measure | Heartbeat, 3-axis acceleration |
| Size | 22mm*30mm |
| Weight | About 4g<br>(w/battery, w/o case) |
| Data Trans-mission | NFC<br>(near field communication)<br>(a.k.a. Wallet Mobile) |

● Image of goal product




Low-power by
Normally-Off Computing

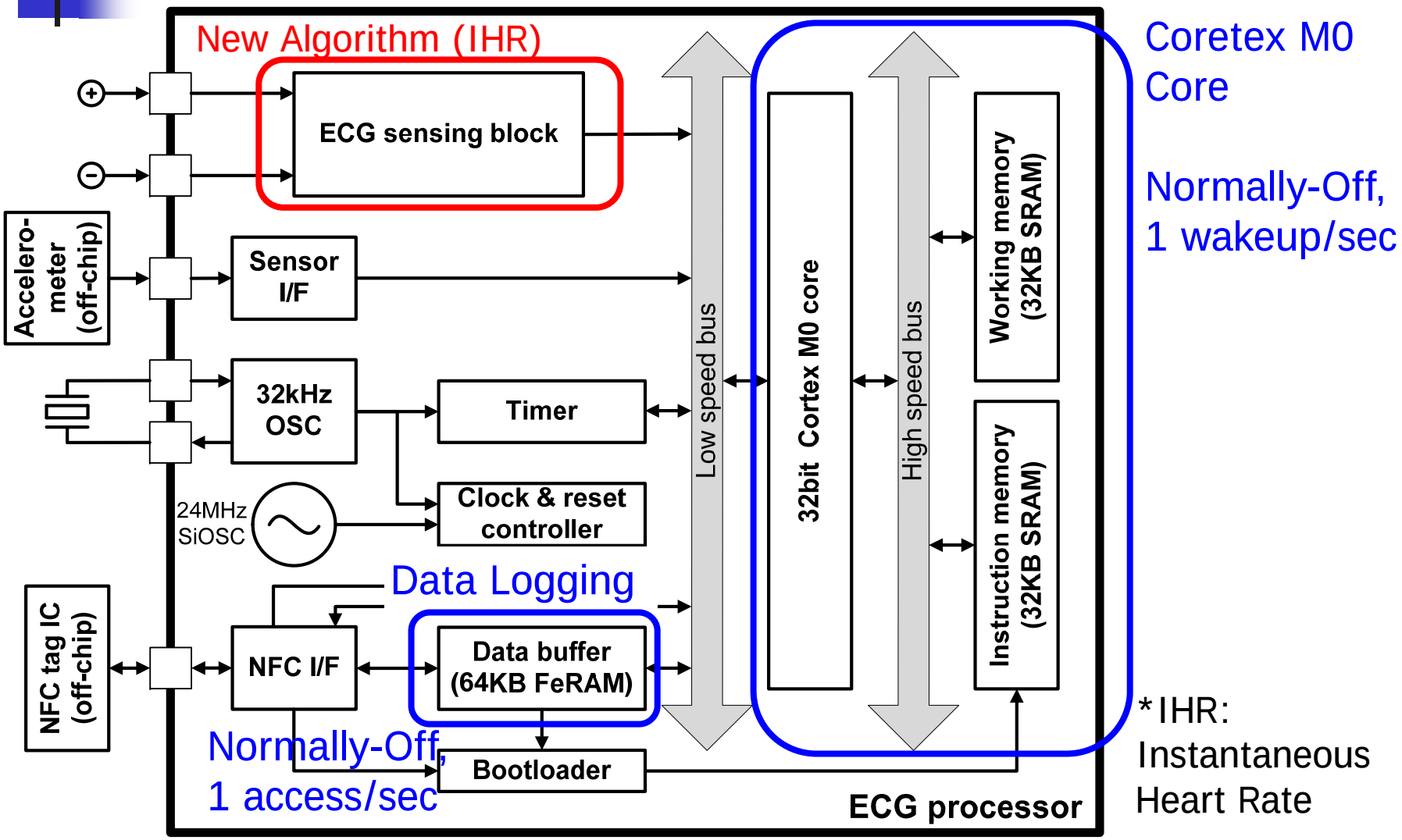
↓

Realize wearable measurement
by light battery and device

↓

Prevention of lifestyle disease

# Block Diagram of ECG Processor

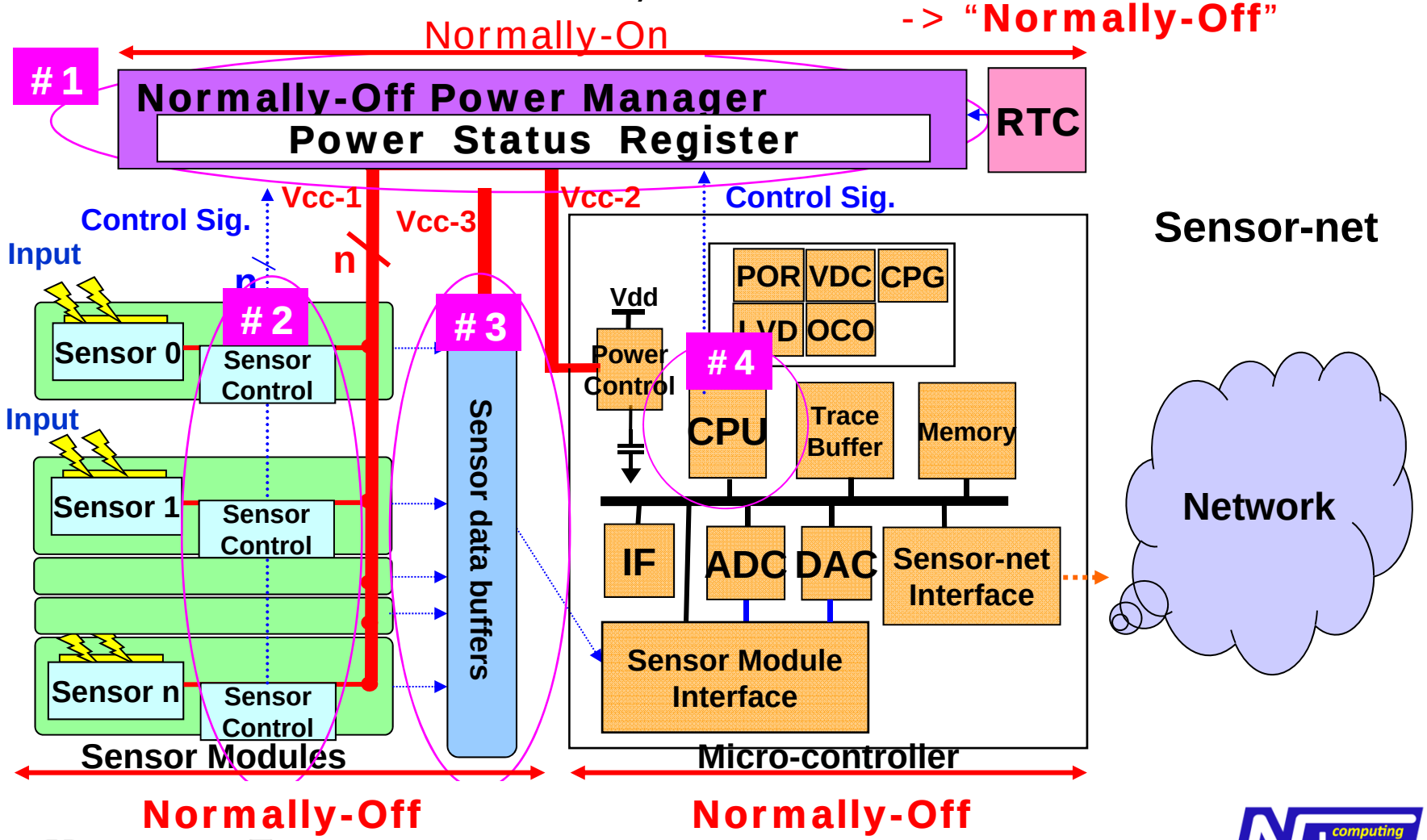



S. Izumi et al., "A 14 µA ECG processor with robust heart rate monitor for a wearable healthcare system," IEEE ESSCIRC, 2013, pp. 145-148

# N-Off Architecture for Low-power Sensor-node (Renesas)

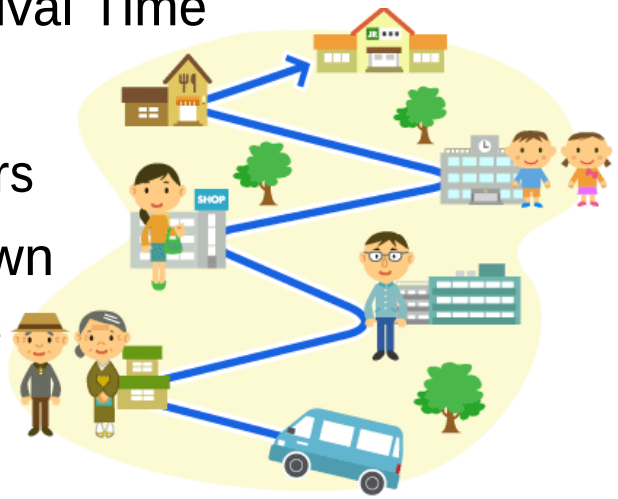
M. Hayashikoshi et.al., "Normally-Off MCU Architecture for Low-Power Sensor Node", IEEE ASP-DAC 2014, Jan. 2014

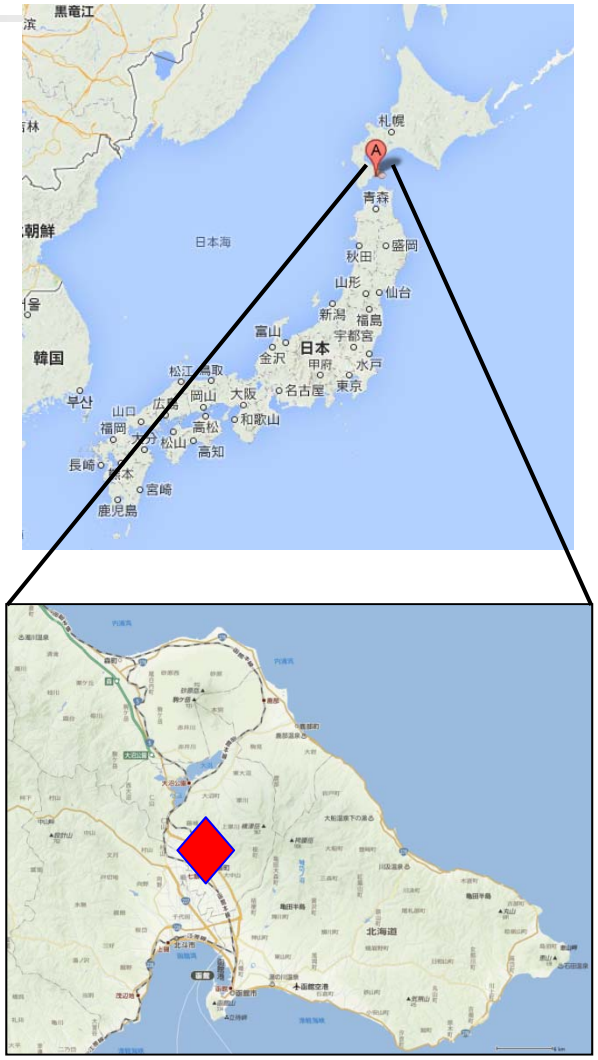
- Sensor-modules are in "Normally-On". -> "**Normally-Off**"
- Microcontroller is in "Normally-On" or "Intermittent". -> "**Normally-Off**"



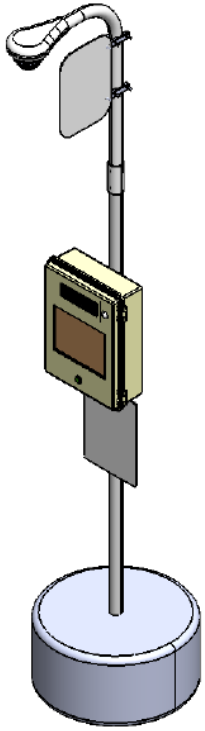
# Field Test of Normally-Off Computing

- Demand Transportation System as an IT-assisted convenient public transportation
  conducted by Renesas Electronics
  - Detection of Demand/User
    - Intelligent Bus Stop
  - Notification of Arrival Time
  - Bus Dispatch
  - Direction to Drivers
  - Test at Nanae Town
    - Area 216.61km$^2$
    - Pop. 28,941



# Intelligent Bus Stop



Interface

- High Load
  - Camera
  - Display
  - WiFi
  - …
- Low Load
  - Pyroelectric sensor
  - Button
  - …

First Prototype Single CPU
→ Heterogeneous CPUs


Bus Dispatched
Expected Arrival
Time 10:45
Just departed XX

# Concluding Remarks

- Opportunities of Normally-Off Computing
  - Intelligent Power Management
  - Non-volatile memory: Potential is extremely high: fast, large capacity, and low power
- Challenges: Temporal Granularity
  - BET is the most important
  - Optimize memory accesses, core activity to meet BET
  - Optimize architecture to make BET longer

  → Co-Optimization of Algorithm, Software, Architecture and Circuit Design is the KEY
- Status on Smart City Applications

  (by Renesas and ROHM)