Evaluating Power-Efficiency for an Embedded Microprocessor with Fine-Grained Power-Gating

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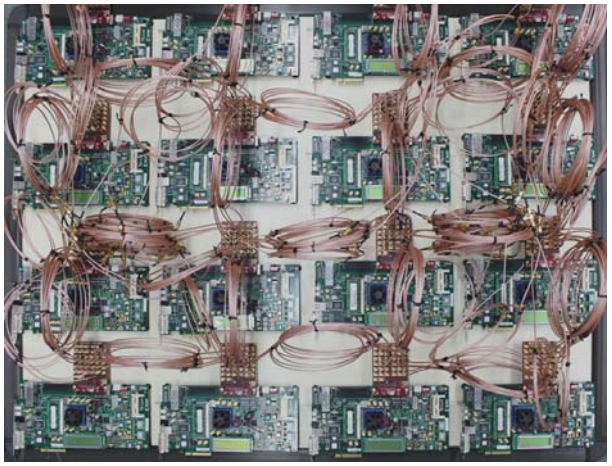
Background

- SMYLEref manycore-processor [1]
  - Manycore SoC architecture &FPGA evaluation environment with 128-cores
  - Processor core: Geyser-3
    - Low-power core with fine-grained power-gating



[1] M.Kondo, “SMYLEref: A Reference Architecture for Manycore-Processor SoCs”, MPSoC’13.

- Leakage power
  - Still occupies non-negligible part of total power consumption even with advanced semiconductor technology
    - 15% - 25% of total chip power according to recently published papers
  - Reduction of runtime leakage-power is important

Introduce fine-grained runtime power-gating capability in Geyser-3

Acknowledgement

- JST-CREST project (2006.10 - 2012.3)
  - *Innovative Power Control for Ultra Low-Power and High-Performance System LSIs*
  - PI: H. Nakamura (U. Tokyo)
  - Co-PI: K.Usami, H.Amano, M.Namiki, T.Kuroda, M.Kondo

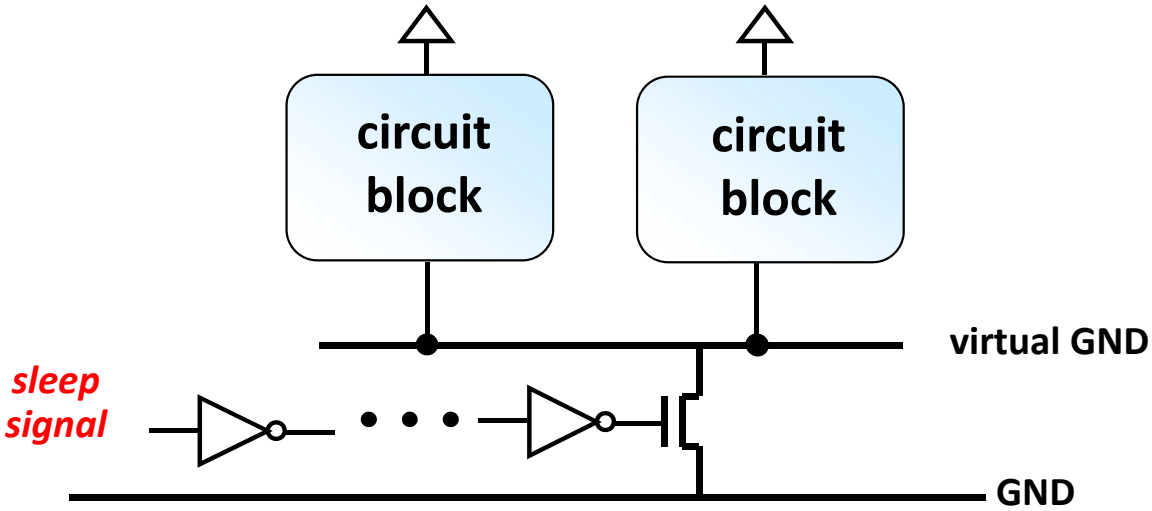
  (JST: Japan Science and Technology Agency)
- Follow-up project: JSPS KAKENHI (S) (2013.4-2017.3)
  - *A Study on Building-Block Computing Systems using Inductive Coupling Interconnect*
  - PI: H. Amano (Keio Univ.)
  - Co-PI: K.Usami, H.Nakamura, M.Namiki, T.Kuroda, M.Kondo

  (JSPS: Japan Society for Promotion of Science)

Power-Gating

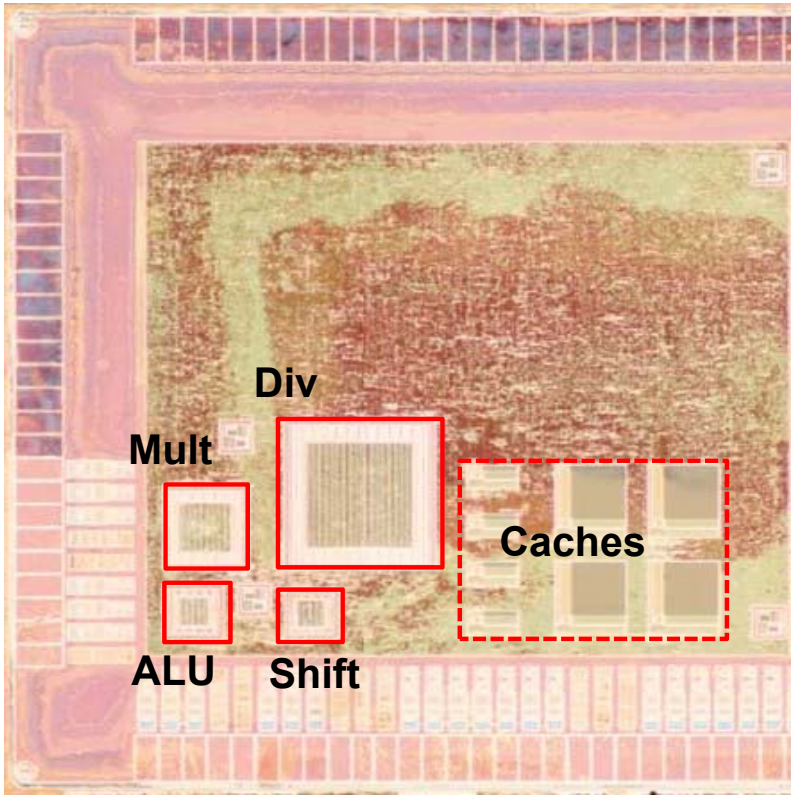
- Power-gating (PG) technique
  - Sleep transistors between GND and NMOS transistors of logics
    - Cuts power-supply to the logic blocks
    - Active/sleep mode controlled by sleep signals

→ *PG can be applied with finer temporal / special granularity*



Chip Implementation of Fine-Grained Power-Gating (Code Name: Geyser-3)

- Proof-of-concept study for Fine-grained power-gating
  - MIPS R3000 compatible embedded microprocessor
  - Target power-gating unit: Functional units (ALU, Shifter, Multiplier, and Divider)
  - Linux successfully operates @ 190MHz

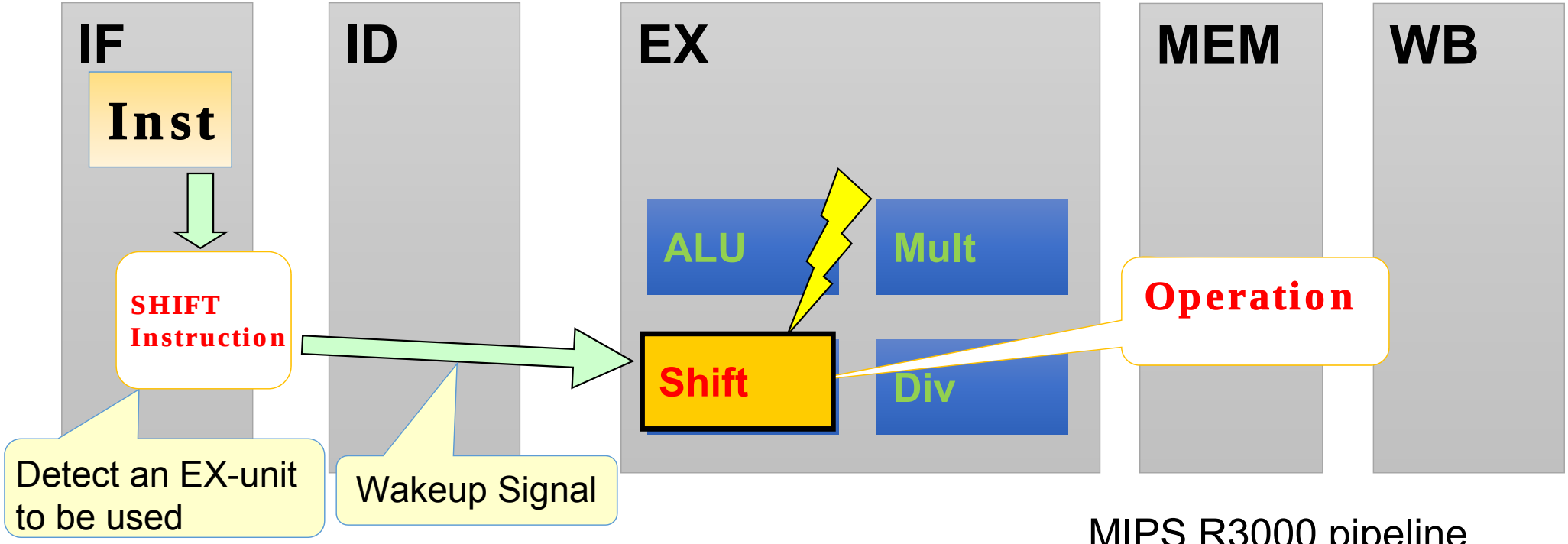


Process Technology	Fujitsu e-shuttle CMOS 65nm,12 metal layers
Area	ALU: 121.4 x 113.4 Shift: 116.4 x 114.8 Mult: 199.4 x 199.4 [um x um] Div: 369.0 x 368.6 Total: 1610 x 1443
Vdd	1.2 [V]
L1 cache	L1-I: 8KB, 64B-line, 2way L1-D: 8KB, 64B-line, 2way
Synthesis	Synopsys Design Compiler
Layout	Synopsys ICC UPF

Basic Power-Gating Functionality in Geyser-3

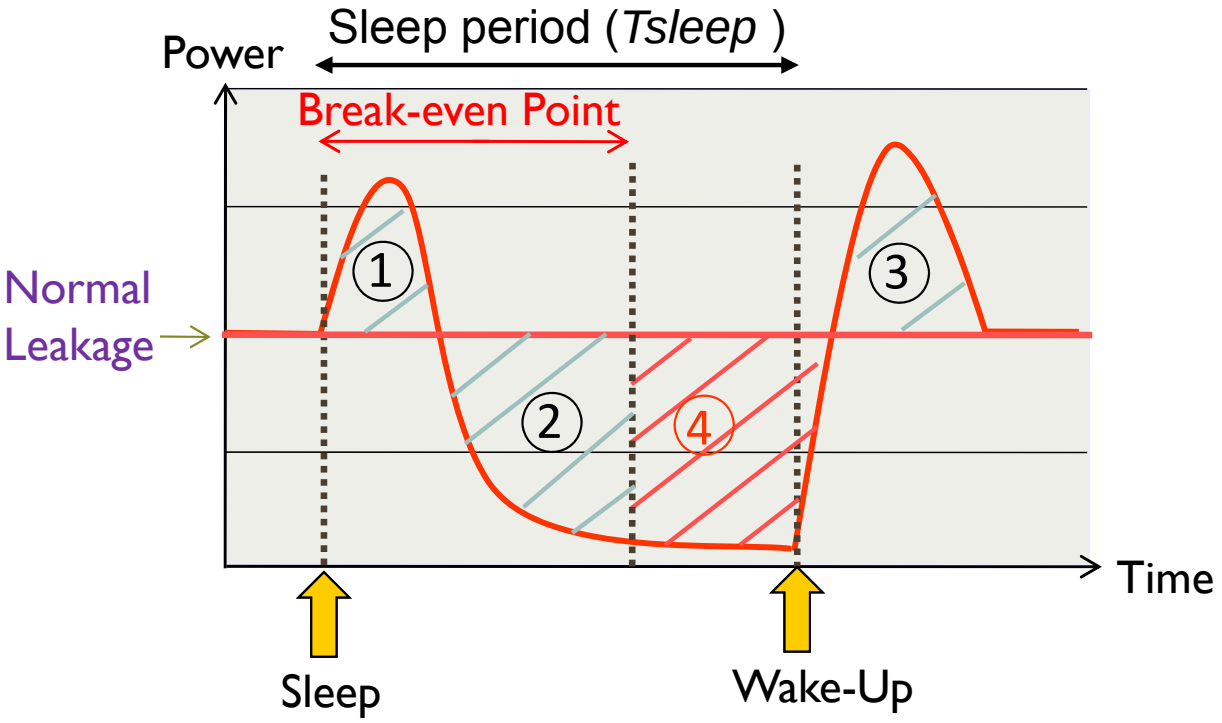
- Hardware-based PG policy
  - Individually control PG for each FU
  - Whenever an FU is in idle, the FU is put to sleep mode
  - Detect and wakeup an FU to be used in IF-stage by pre-decoding

  → one-cycle time margin for the wakeup



MIPS R3000 pipeline

Energy Overhead of Power-Gating



①+ ③ : Energy overhead

② : part of leakage saving

①+ ③= ②

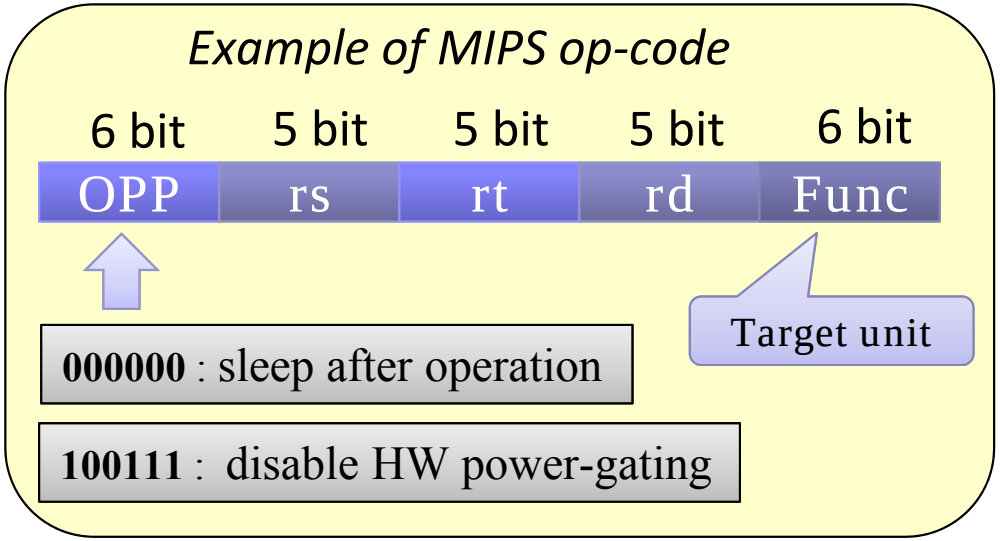
Break-Even Point (BEP)

④ : Net Energy saving

- If *Tsleep* > BEP : reduction of energy consumption ☺
- If *Tsleep* < BEP : increase in energy consumption ☹
- Needs "guard" mechanisms to avoid negative benefit of PG

Compiler Support for PG Control

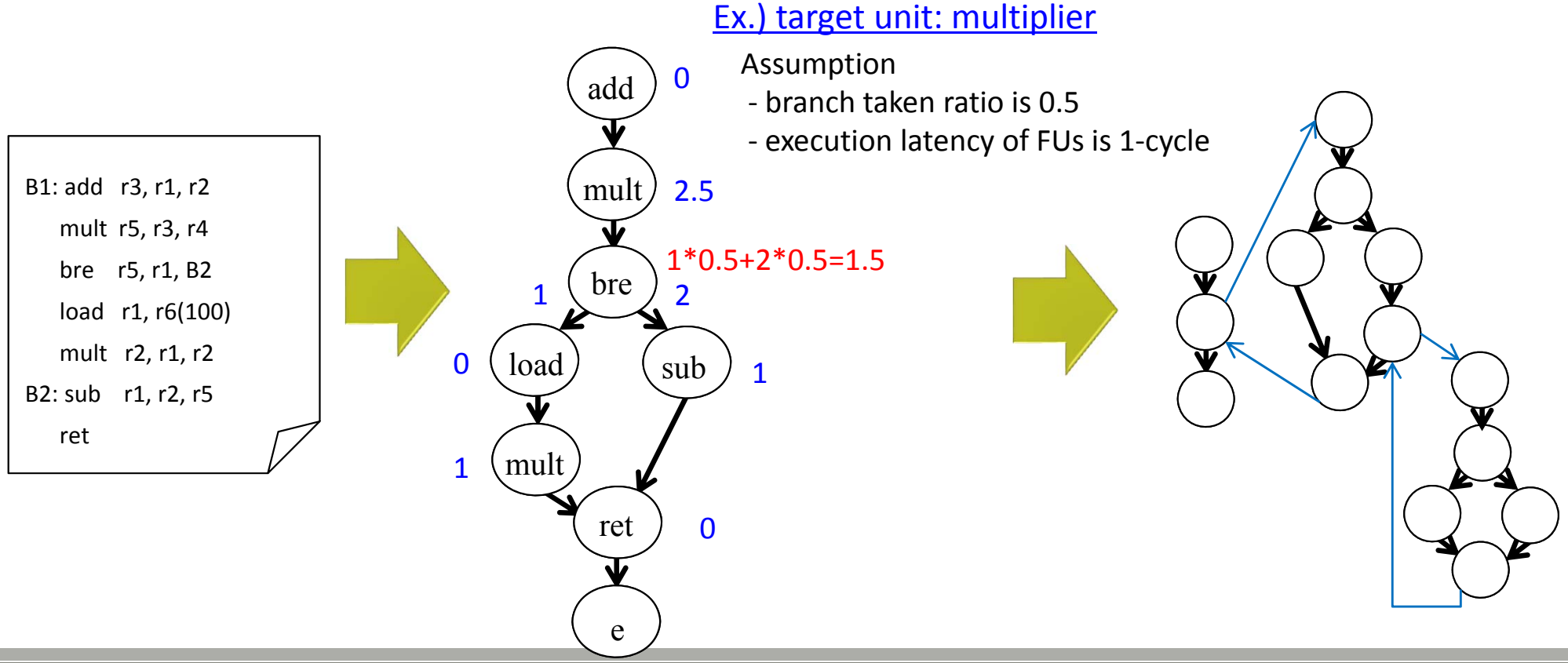
- Compiler support
  - Compiler disables hardware-based PG instruction-by-instruction
  - Based on expected idle period and BEP
- ISA extension
  - Assign unused opcode for disabling hardware-PG
    - → binary-compatible with MIPS processors



- Code generation
  - If predicted idle period for each instruction is less than BEP, use special opcode for disabling HW-based PG functionality
  - Otherwise, normal PG

Compiler Guided Idle Cycle Prediction

- Prediction Steps
  1. Generate CFG from assembly code
  2. For each node, estimate the period between current node and node which uses the target FU (based on data-flow analysis technique)
  3. Pass idle cycle info. between procedures (interprocedural analysis)



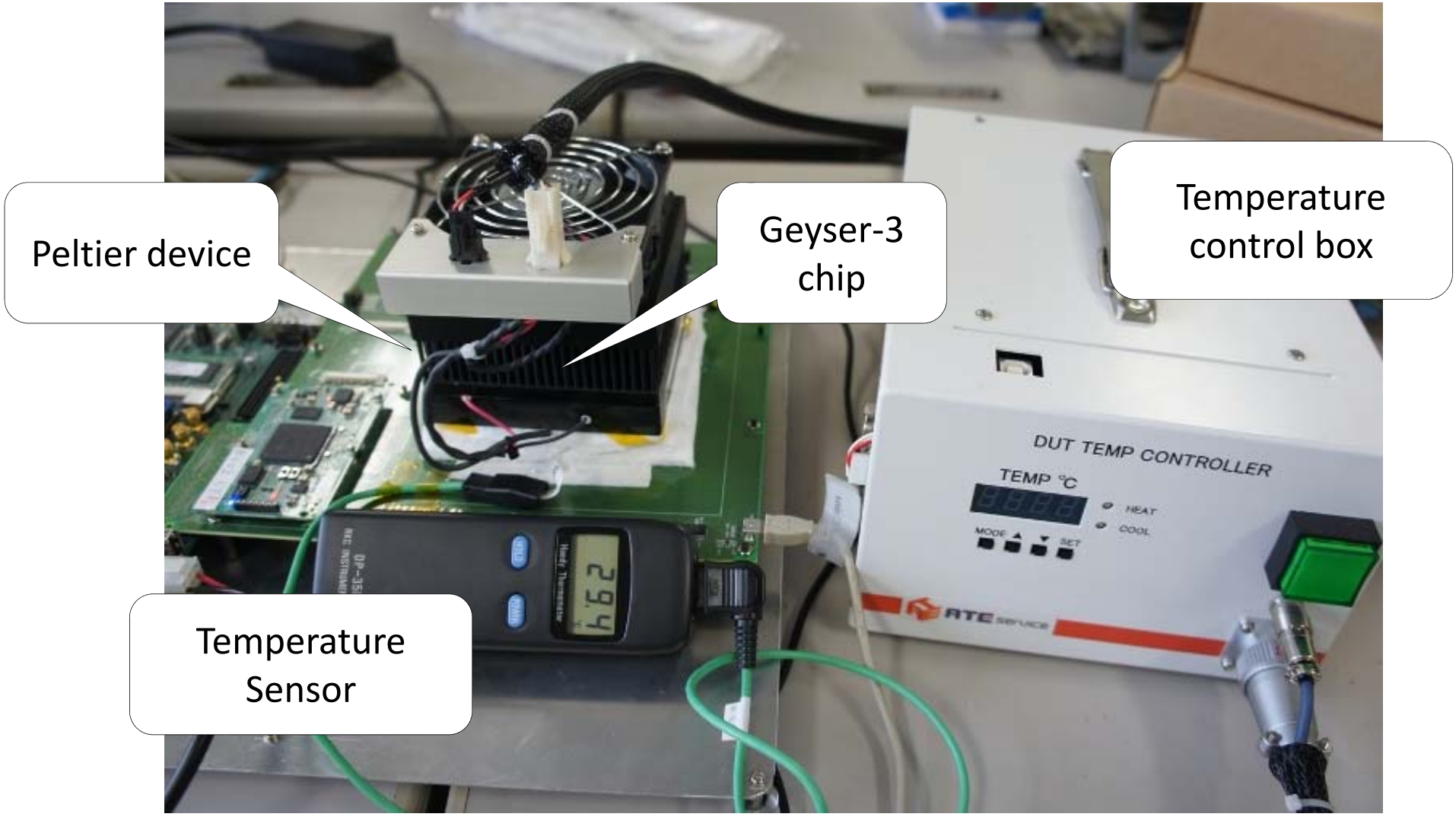
Evaluation

- Evaluate FUs' power supply domain
  - Electric-current sensor measures the electric current every 33ms
- Configuration
  - Core clock frequency: 40MHz (due to board I/O limitation)
  - Benchmark: several programs from MiBench
  - gcc soft-float functionality for floating-point operations
  - Ambient temperatures: 25C and 55C
- Assumed BEP (cycles) for code generation

	ALU	Shift	Mult	Div
BEPset (for 25C)	56	47	28	11
BEPset (for 55C)	21	21	11	4

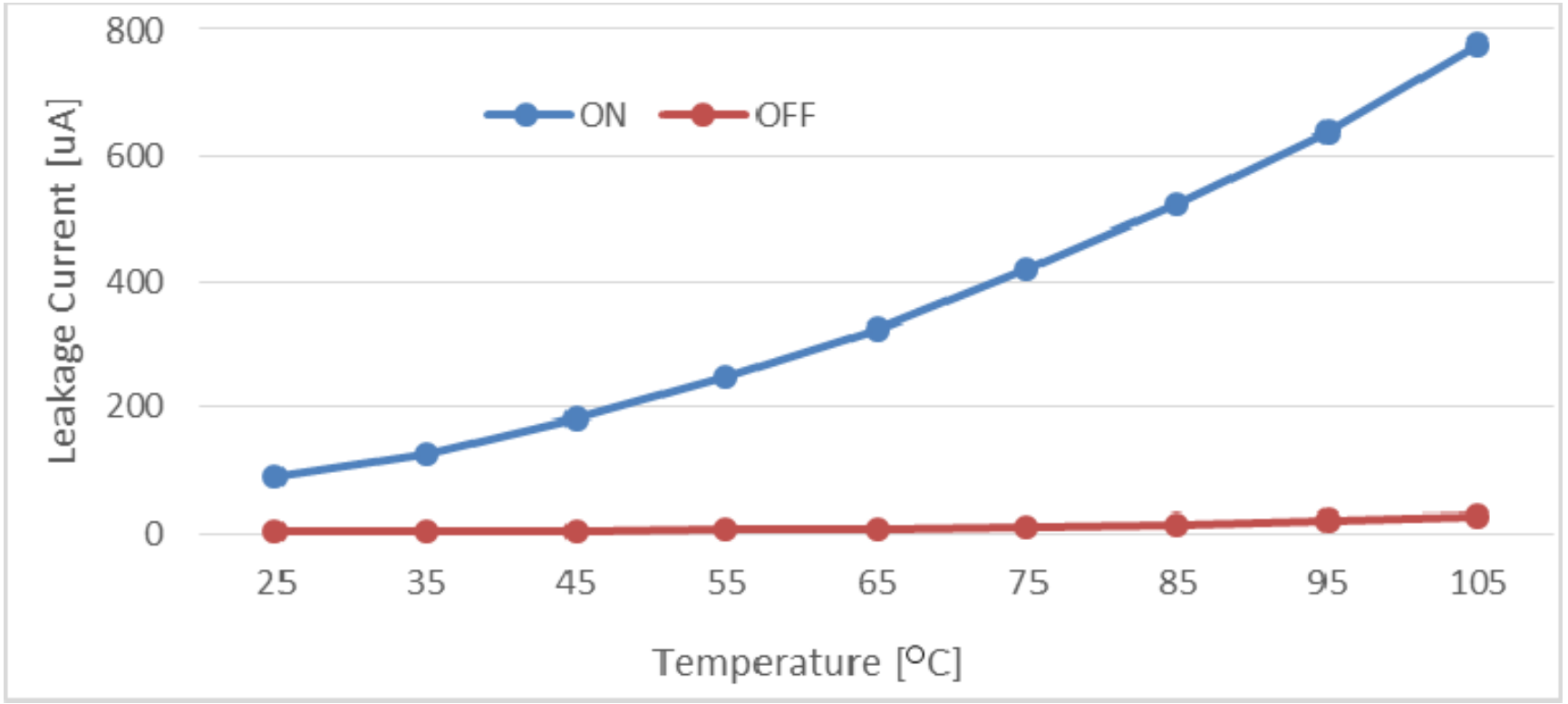
Evaluation Environment

- Chip temperature control facility



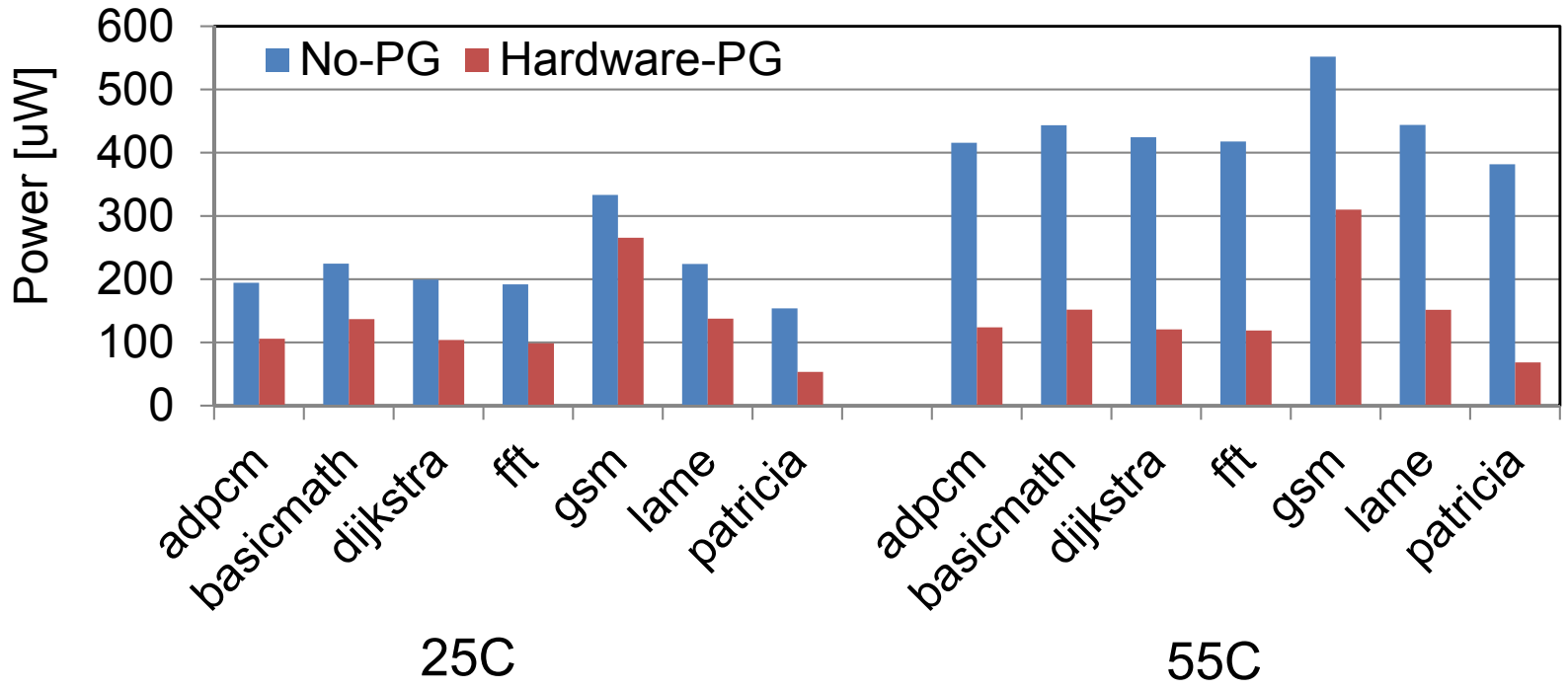
Basic Power-Gating Performance of Geyser-3

- All FUs are statically powered-on (ON) vs. powered-off (OFF)
  - Clock signal is stopped to exclude dynamic power
- About 97% of leakage current reduction



Evaluation Result (1/2)

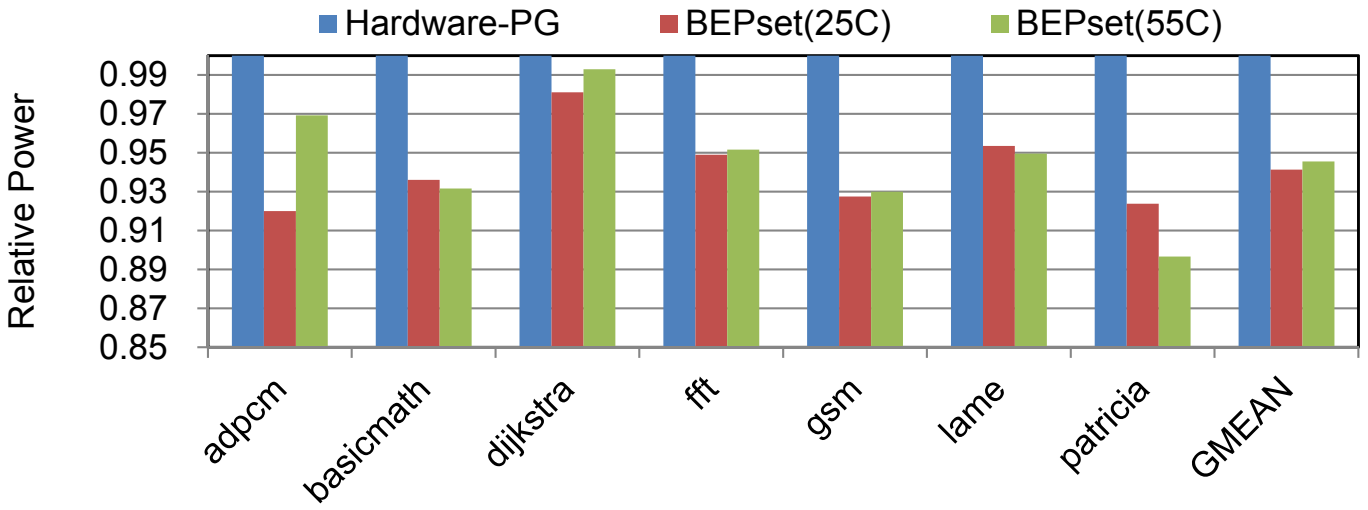
- Power reduction by hardware-based PG scheme
  - Power consumed in FUs (including dynamic power)
  - Significant power reduction
    - On average, 44% for 25C and 67% for 55C



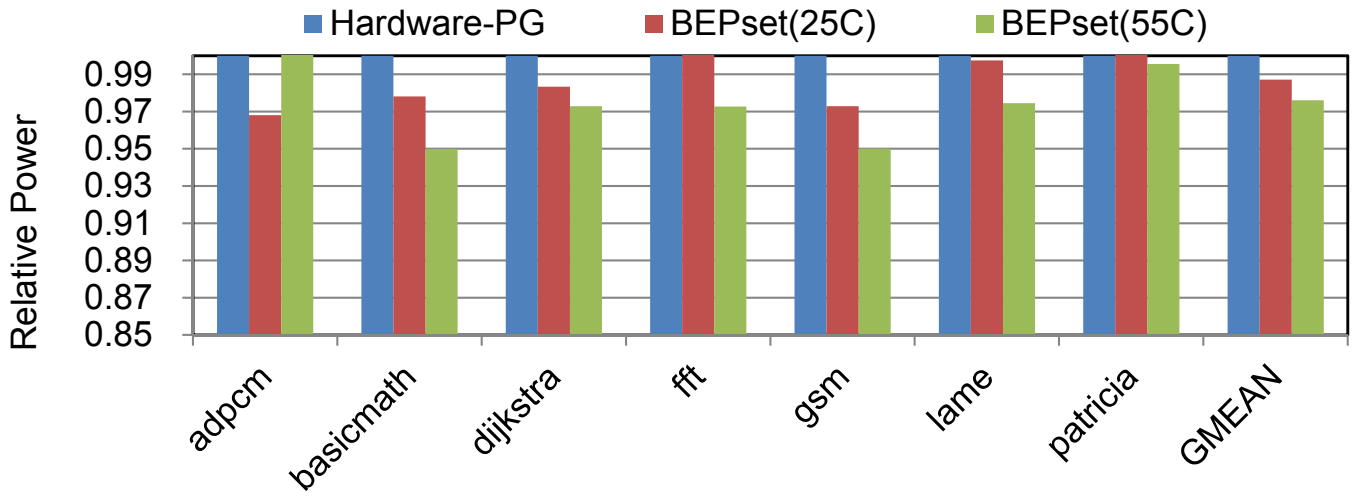
Evaluation Result (2/2)

- Effect of compiler support
  - Save more power by compiler cooperated PG

Core temp. = 25C



Core temp. = 55C



Summary

- Geyser-3
  - MIPS R3000 like processor core
  - Used in SMYLEref manycore-processor
  - Run-time fine-grained power-gating for leakage-power reduction
- Evaluation of fine-grained power-gating in Geyser-3
  - Compiler support for power-gating management
  - 47% - 67% of power reduction
  - Additional 5.9% more power saving with compiler support
- Future work
  - OS support for dynamic object code management
  - Evaluate power efficiency in manycore environment

Thank you!