Low-Power Processor Solutions for Always-on Devices

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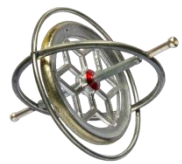
ARC Synopsys

Always-on Mobile Devices

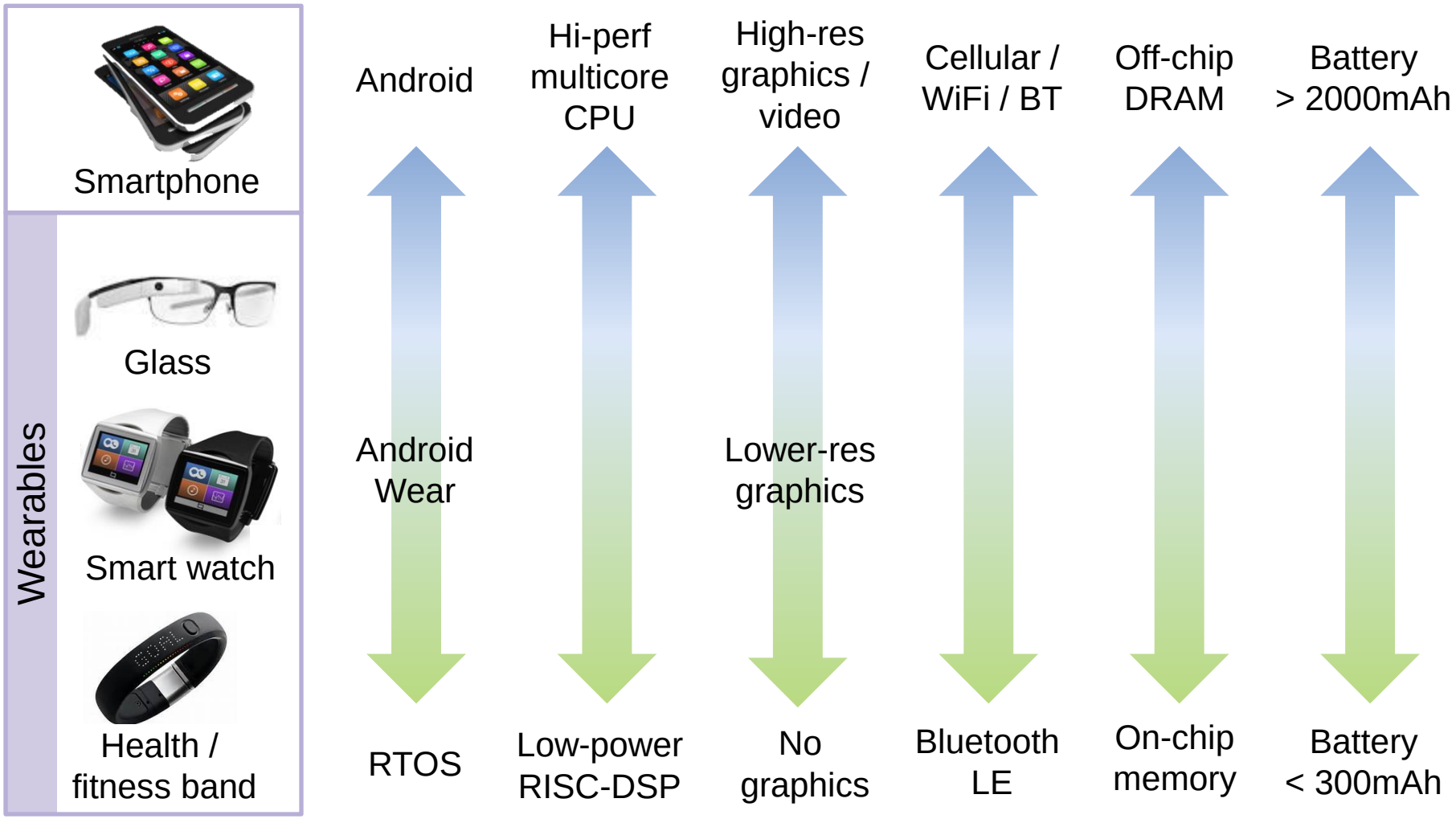
Mobile devices on the move

- Mobile devices are becoming context-aware
  - Use sensors to monitor movement, heart rate, sound, etc.
- Enables new applications
  - Smarter mobile devices performing new functions
  - Changes the way users interact with the devices
- Always-on
  - Always listening
    - Microphone input — Voice activation
  - Always watching
    - Camera input — Face activation, wake-on-gesture
  - Always sensing
    - Sensor input — Motion sensing, health & fitness monitoring
  - Always connected
    - Wireless links — Cloud data push services, Bluetooth LE



Always-on Mobile Devices

Devices with different characteristics



Always-on Mobile Devices

Processors for always-on processing

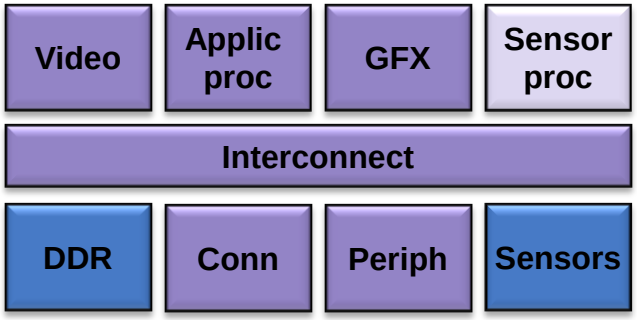
Smartphone

Wearables

Glass

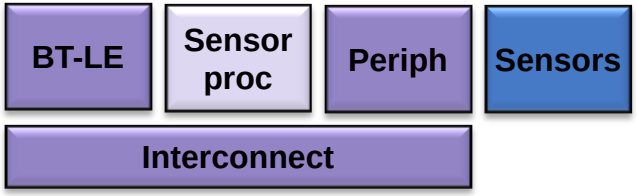
Smart watch

Health / fitness band



Processor for always-on

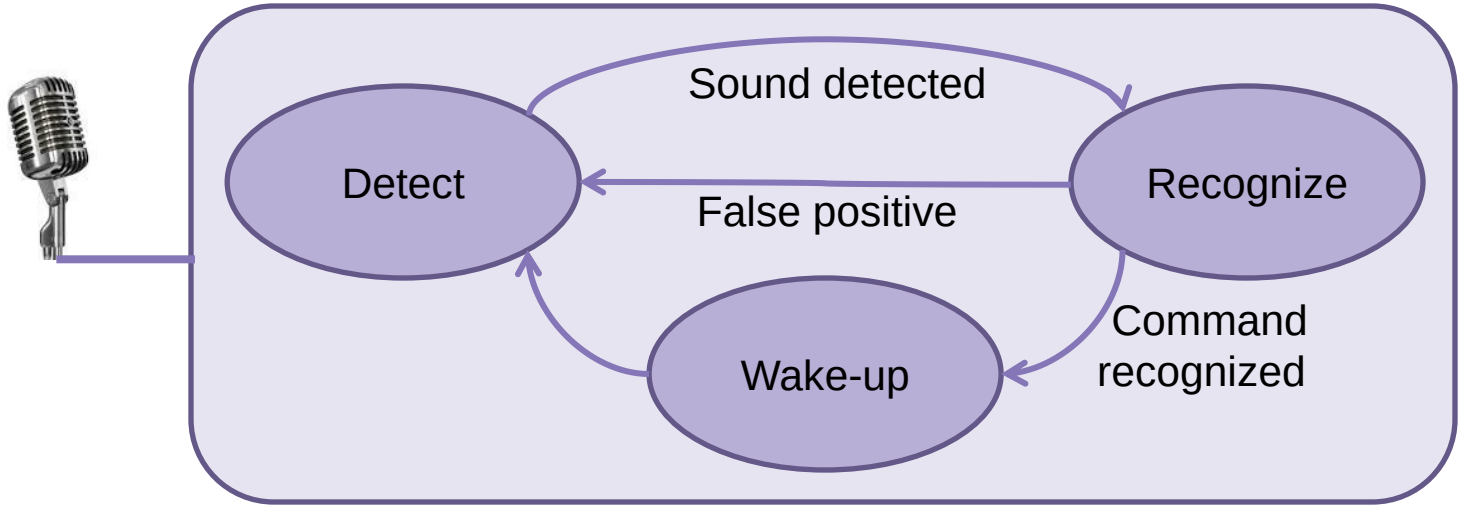
- Operate in different SoC contexts
- Fmax typically < 100 MHz
- Lowest power in each mode
- Mixed control and DSP



- **Separate core for always-on processing**
  - Wake-up application processor only when needed
- **Low power**
  - > 10x lower power than application processor
  - Battery in wearable needs to last weeks
- **Multiple modes**

  E.g. voice activation:
  - Standby / detection mode
  - Recognition mode
- **Mixed control and DSP**
  - DSP for processing of sensor inputs

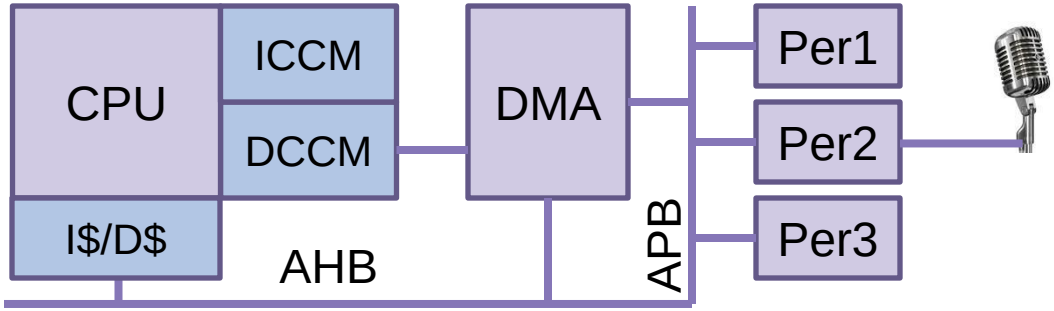
Voice Activation



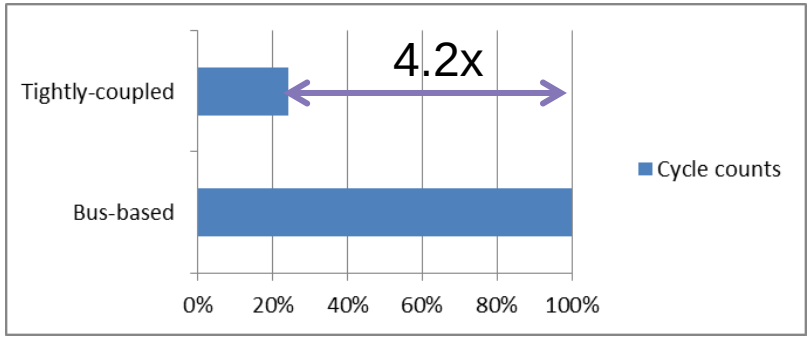
- Detect
  - System mostly resides in detect state, needs lowest power
  - Very light workload (< 1 MHz)
- Recognize
  - Activated when sound is detected
  - Applies DSP algorithms to recognize voice command(s)
  - Higher workload (5 – 10 MHz for single phrase recognition)
- Wake-up
  - Trigger action in application

Memory Configurations

Closely coupled memories



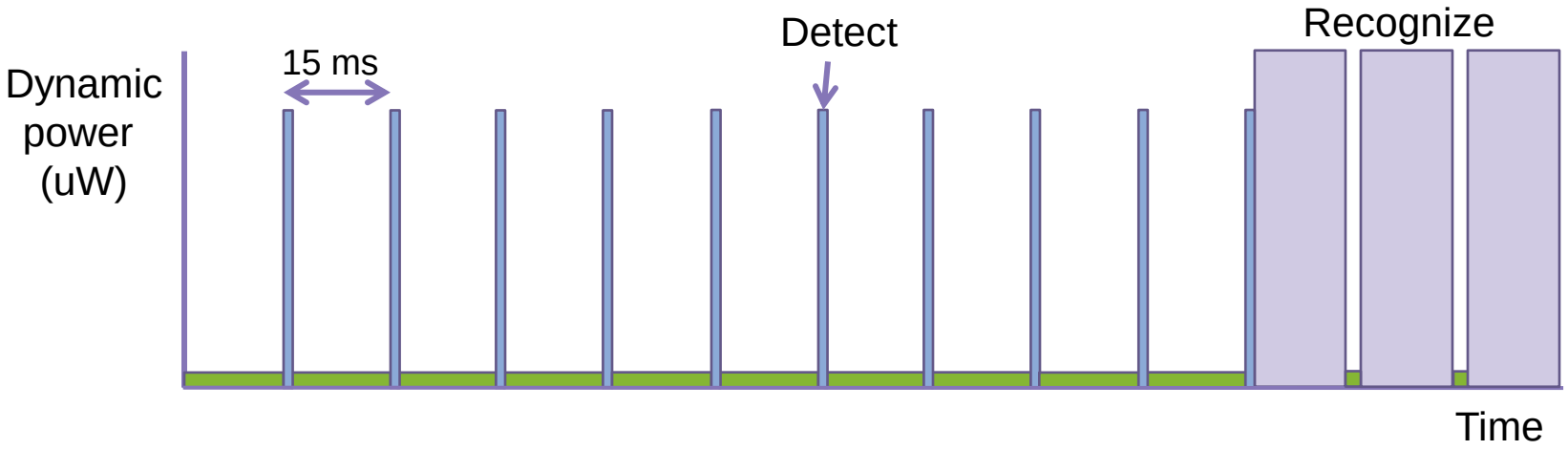
- DMA stores data in DCCM while processor sleeps
- DMA wakes up processor when buffer available
- After wake-up, processor does not have to access data over AHB bus
  - No energy spent in bus accesses
  - Lower latency → processor can run at lower frequency



- Sensor hub application
- Analysis of processing stage
- Core and bus at same frequency
- Bus-based with instruction fetch queue

Voice Activation

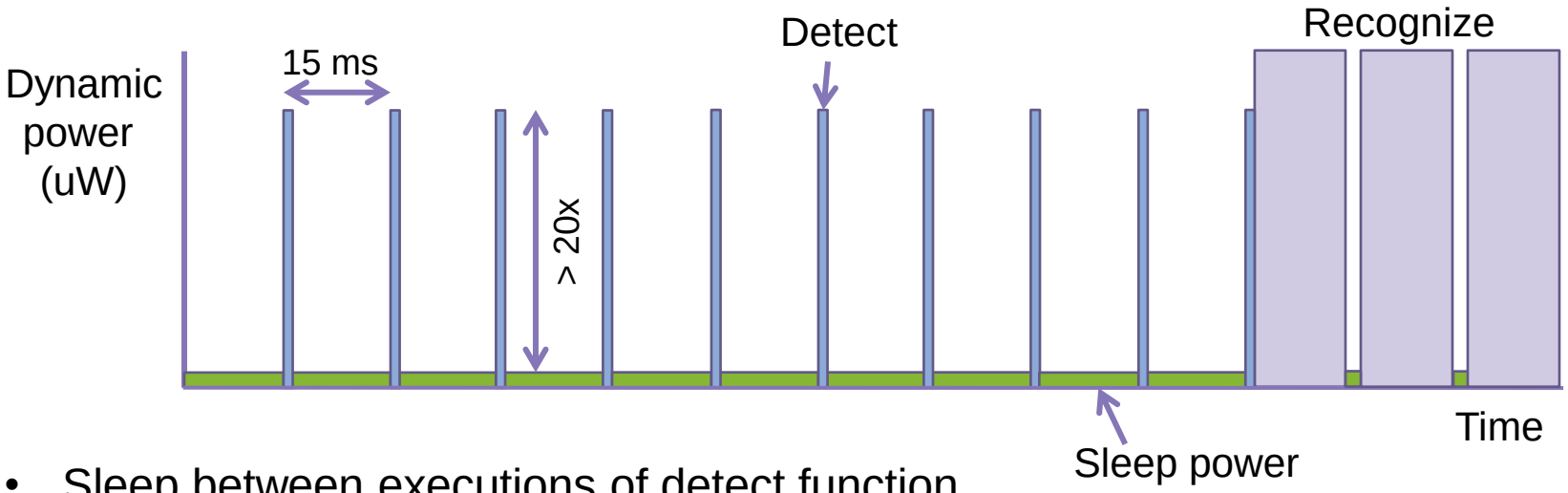
Power management



- Voice activation detect mode
  - At 10 MHz processing duty cycle < 2.5%
- Opportunity for energy savings
  - But need to allow access to DCCM for DMA
  - Would be no different with memory on AHB bus

Voice Activation

Power management



- Sleep between executions of detect function
  - Fast sleep and wake-up
  - Low sleep power → simple and effective
- Frequency scaling
  - Saves sleep power (only)
  - Requires clock domain crossings
- Voltage switching
  - Saves leakage power as well
  - Requires switch, clamps, data retention, PMU

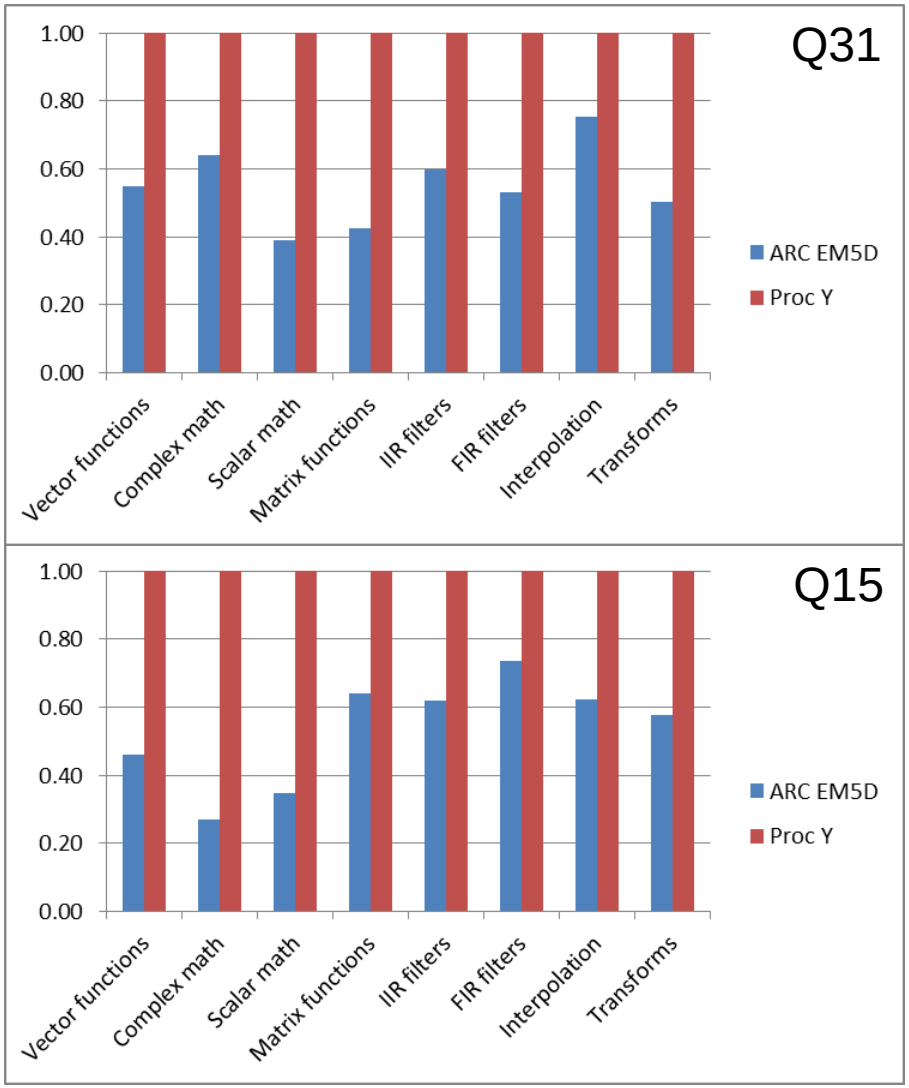
Instruction Set Architecture

- It's all about ~~power~~ energy
  - Minimize energy per function → power x cycles
- Mixed control and DSP
  - Good power and efficiency for RISC and DSP
- Code size
  - Memory footprint, active memory power, I-cache miss rate
- Data types
  - Fractional Q31, Q15, Q7
- DSP instructions
  - MUL/MAC operations
  - Rounding & saturation
  - Vector operations 2x16 & 4x8
  - Complex (16+16)x(16+16)
  - Vector unpacking

- Vector 16x16 MAC
  - acc.lo += a.lo * b.lo
  - acc.hi += a.hi * b.hi
- Dual 16x16 MAC
  - Inner-product style
  - acc += a.lo * b.lo + a.hi * b.hi

Energy Consumption

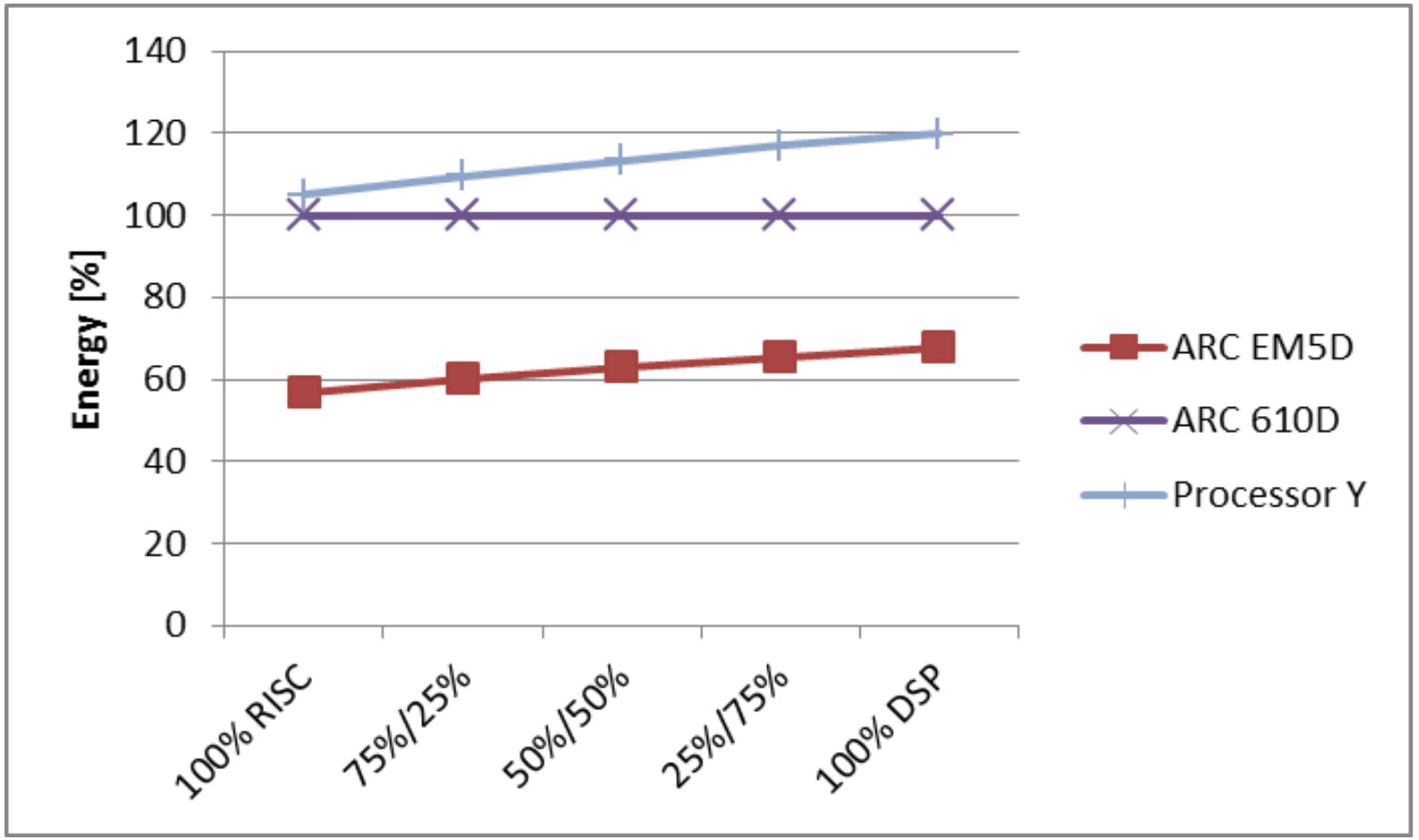
For DSP workloads



- Energy consumption for categories of DSP functions
  - Logic dynamic *energy*
  - For Q31 & Q15 DSP functions
- Small code size
  - Code size Q31: 57%
  - Code size Q15: 89%
- Low power implementation
  - Unified MUL/MAC unit
  - Aggressive clock gating
  - Operand gating / isolation
- Configurability & extensibility

Energy Consumption

For RISC and DSP workloads

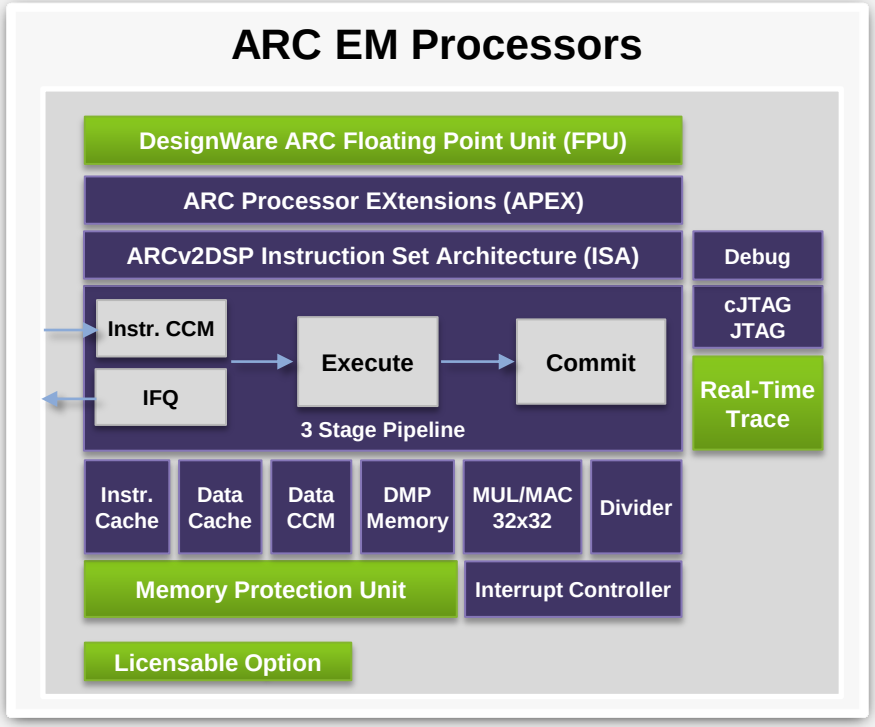


Note: energy consumed for executing fixed workloads

ARC EM Processors

Combining High Efficiency Control & Digital Signal Processing

Power & Area Efficient Processors based on Extensible ARCv2DSP Architecture



EM5D	Up to 2MB Instruction and Data CCMs
EM7D	I & D CCMs plus I & D Caches (up to 32K)

- ARCv2DSP ISA adds over 100 new DSP-focused instructions
  - Vector/SIMD, Matrix, Saturating & Complex
  - Configurable DSP hardware features
- New EM5D & EM7D cores optimized for ultra low-power control and DSP
  - Energy-efficient 3-stage RISC pipeline
  - Unified single cycle 32x32 MUL/MAC unit
  - Energy-efficient signal processing of voice/speech, audio and sensor data
  - Optional Floating Point Unit (SP & DP)
- Easy software development with rich DSP software library & C/C++ Compiler

Conclusions

- Need to optimize at all levels for low energy
  - Efficient ISA for mixed control and DSP
  - Energy efficient access to memories (CCMs)
  - Low power hardware implementation (clock & operand gating)
  - Effective sleep modes
  - Configurability and extensibility
- Significant energy reductions can be achieved
  - Good application fit is key
  - Good design choices matter
- Flexibility is key to fit in different SoC contexts
  - Memory architecture
  - Power management schemes


Thank You
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