Ageing Assessment, Prediction, and Lifetime Reliability Aware Resource Management

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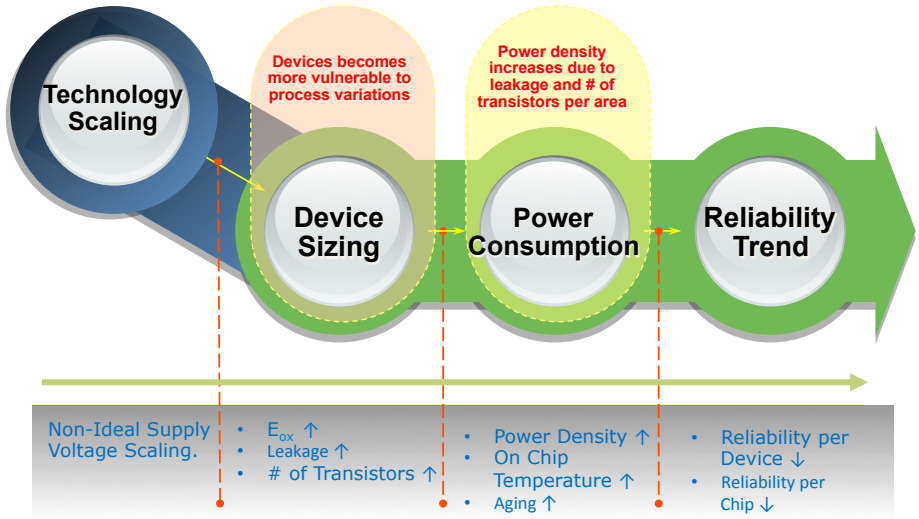
Agenda

1. **Introduction**
2. Challenges
3. DRM System
4. DRM Implementation
5. Conclusion

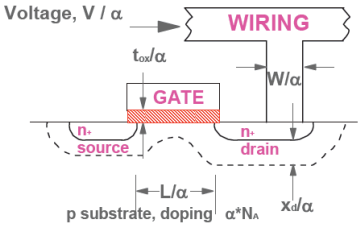
Why Reliability Became an Issue?

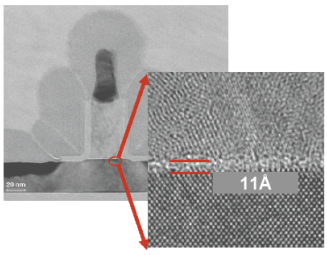


What Scaling Means?

Non-Ideal Scaling

CMOS Scaling Rules





SCALING:

Voltage:	V/α
Oxide:	t_{ox}/α
Wire width:	W/α
Gate width:	L/α
Diffusion:	x_d/α
Substrate:	$\alpha * N_A$

R. H. Dennard *et al.*, *IEEE J. Solid State Circuits*, (1974).

RESULTS:

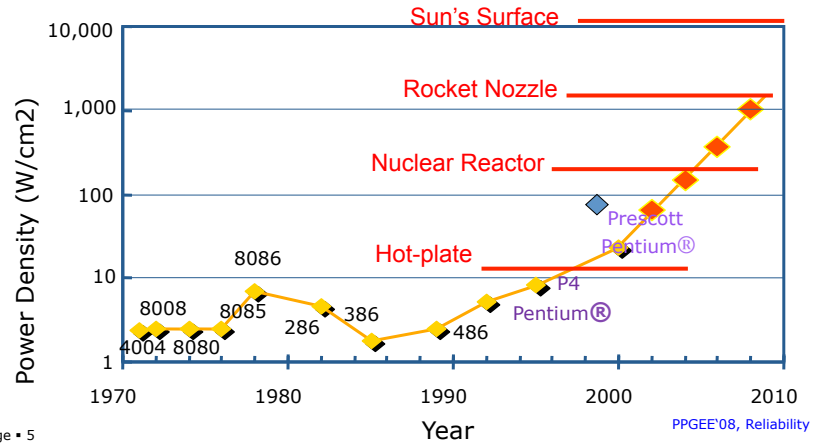
Higher Density:	$\sim\alpha^2$
Higher Speed:	$\sim\alpha$
Power/ckt:	$\sim 1/\alpha^2$
Power Density:	~~Constant~~

- Approaching atomistic and quantum-mechanical boundaries
- **Atoms are not scalable!**

Chen IBM 2006

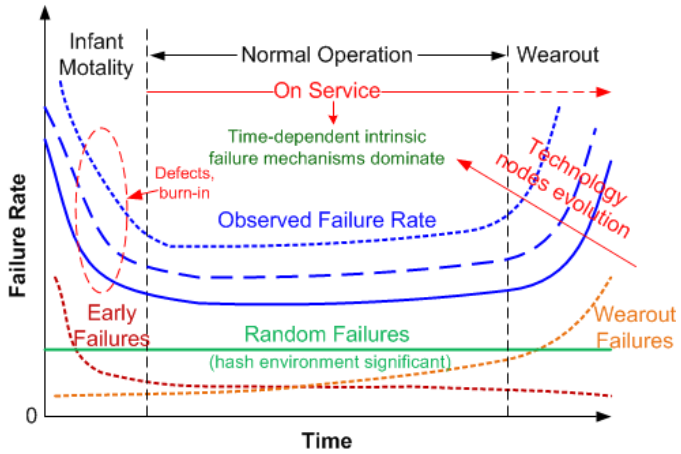
Power Density

Ever *increasing power* density leads to high temperature in chip, which accelerates temperature-elevated intrinsic failure mechanisms, like NBTI.



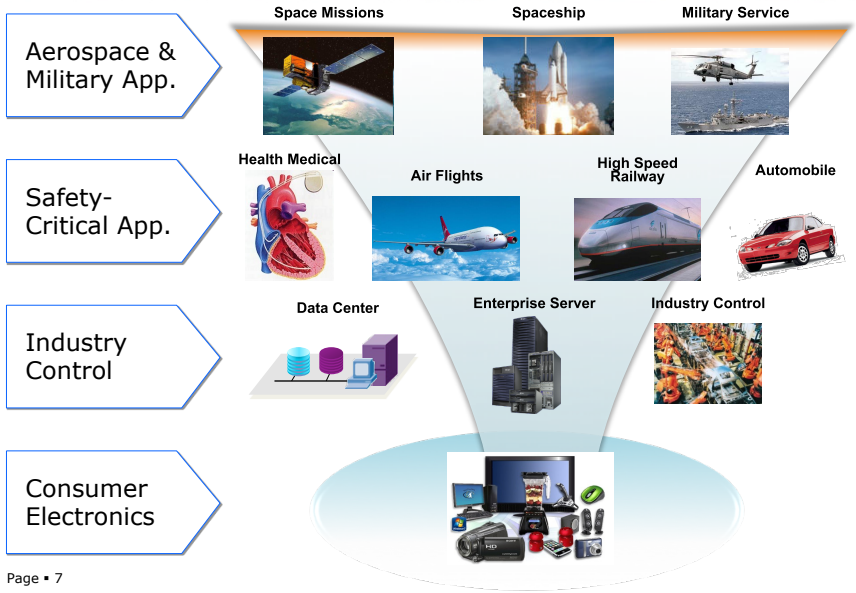
Reliability vs. Technology

Device wear out is clearly observed and also End-of-Life approaches faster as technology advances.



"Bathtub" Curve of Reliability for Different Technology Generations

Reliability is Important for…



Page ▪ 7

Small Failures May Cost a Lot!

A small leak may sink a great ship.

http://telstarlogistics.typepad.com/telstarlogistics/2008/08/photos-and-vide.html

- B-2 bomber crash in Guam 2008
  - **$USD 1.4B loss**
- ***3 air data sensors malfunction***, moisture in the transducers during calibration distorted the information in the air data system.
- This caused the flight control computers to calculate inaccurate airspeed and negative angle of attack upon takeoff.

Page ▪ 8

Agenda

1. Introduction
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4. DRM Implementation
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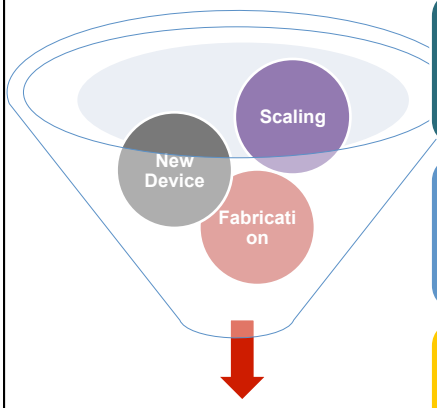
Page ▪ 9

Reliability Becomes More Difficult



Scaling
- Device dimension decrease continuously, physical limit is approaching.

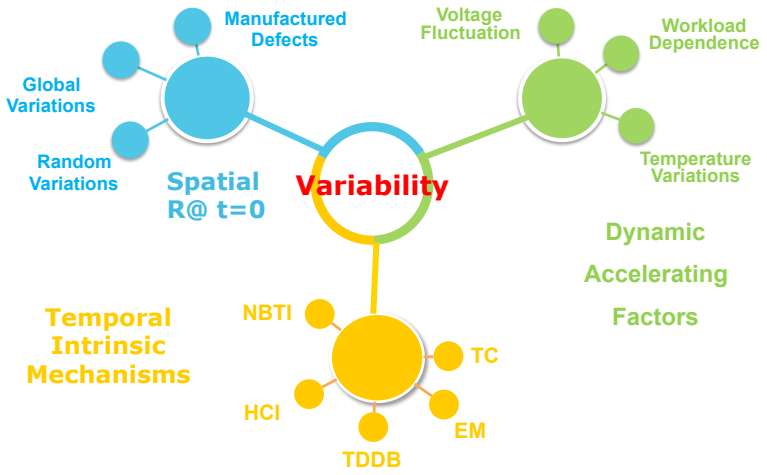
New Device
- New device structures and materials introduces new reliability concerns.

Fabrication
- Manufacturing variability increases since process geometries gets smaller, optical diameter doesn't decrease proportionally.

Page ▪ 10

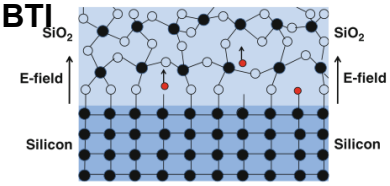
Reliability Challenges

The most reliability challenges come from **Variability**, which can be further divided into three categories: ***spatial***, ***temporal***, and ***dynamic*** variability.



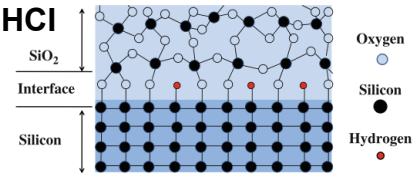
Failure Mechanisms

NBTI



- Holes from the inversion layer tunnel into the gate oxide, break the Si-H bonds and leave behind interface traps.
- Hydrogen diffuses away from the Si/SiO2 interface.

HCI

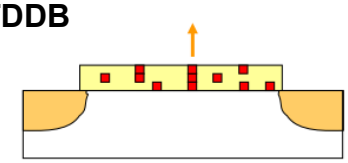


- " Lucky electrons" gain enough energy while drifting across the channel.
- The "hot" electrons produces interface damage in a localized region near the drain end.

- NBTI and HCI creates hole traps at Si/SiO2 interface and in the oxide, which leads a positive shift of $|V_{th}|$ to the device;
- NBTI and HCI highly depends on the stress probability at the device;
- Furthermore, NBTI and HCI are prone to voltage fluctuation and temperature variations.

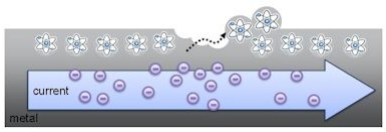
Failure Mechanisms – Cont'd.

TDDB



- The gate oxide breaks down as a result of long-time application of relatively low electric field.
- The breakdown is caused by formation of a conducting path through the gate oxide to substrate due to electron tunneling current, when MOSFETs are operated close to or beyond their specified operating voltages.

EM



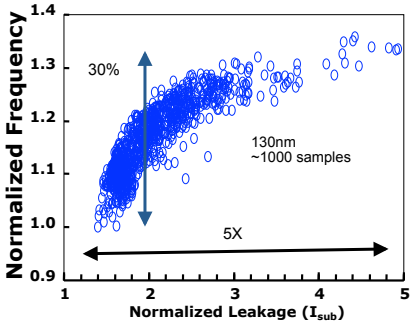
- Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms.
- As the structure size in ICs decreases, the practical significance of this effect increases.

- TDDB and EM are discovered and well studied for quite a long time, but with decreasing oxide thickness and metal width, they could be still troubles;
- The breakdown of these failure mechanisms is progressive, but the damage can be permanent as effects accumulates.

Page ▪ 13

Process Parameter Variations

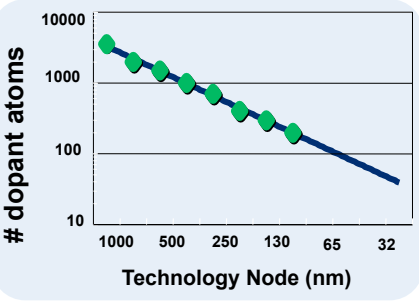
Source: Intel



Delay and Leakage Spread

Frequency ~30%
Leakage Power ~ 5-10X

Source: Intel



Random dopant fluctuation

Device parameters are no longer deterministic!

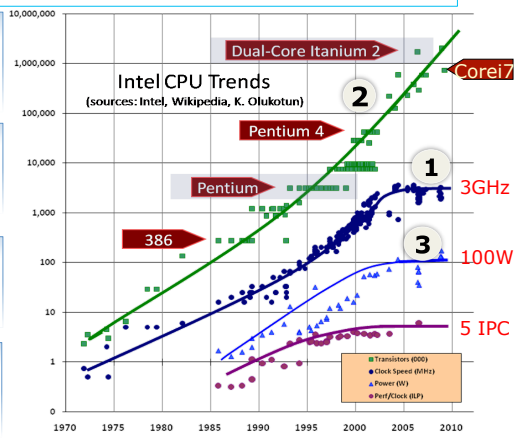
Page ▪ 14

As Scaling Continues…

Multi/Many core processor is more power efficient, and give more flexibility to perform DRM with graceful degrading policy!

1. **Clock Frequency**
   Fixed or getting slower.
2. **# of Transistors per Chip**
   Doubles every 18-24 months.
3. **Power per Chip**
   Reaches almost maximum.

Moore's Law
Reinterpret to *# of transistors or cores per chip*.



From K. Olukotun, L. Hammond, H. Sutter, and B. Smith

Agenda

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2. Challenges
3. **DRM System**
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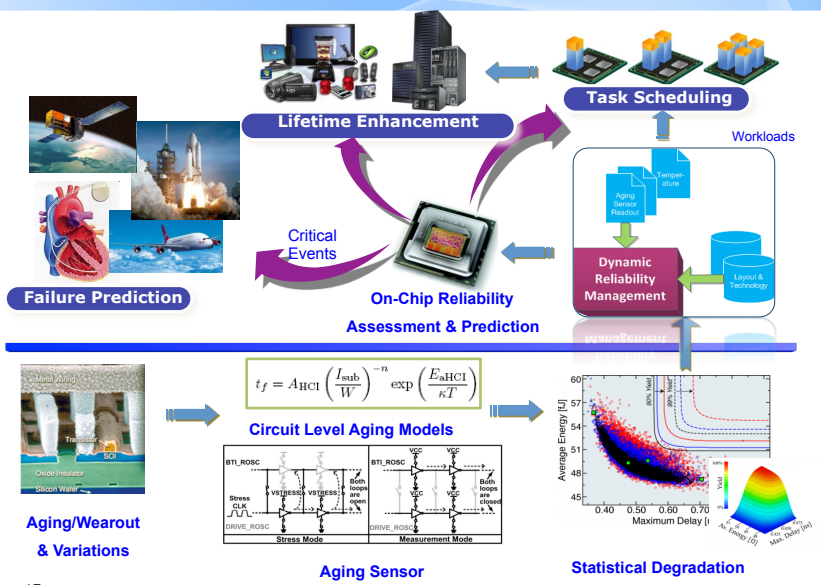
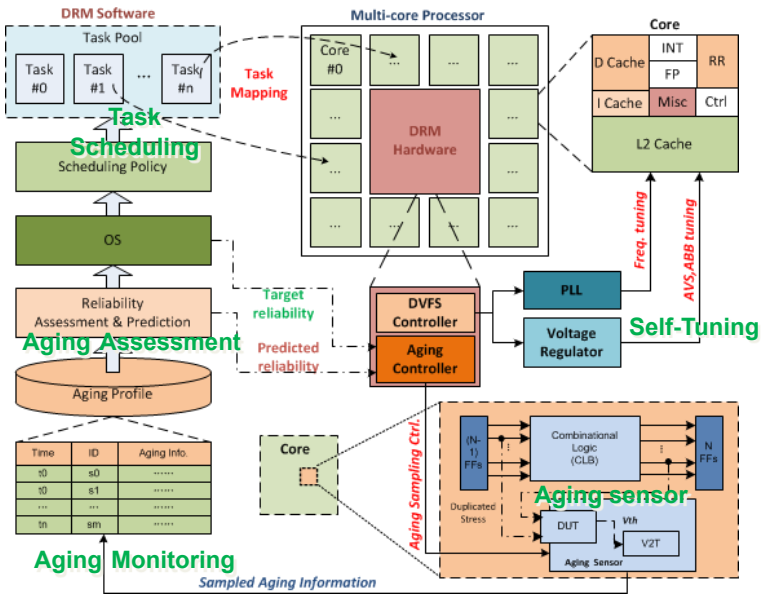
DRM Concepts & Applications



Page ▪ 17

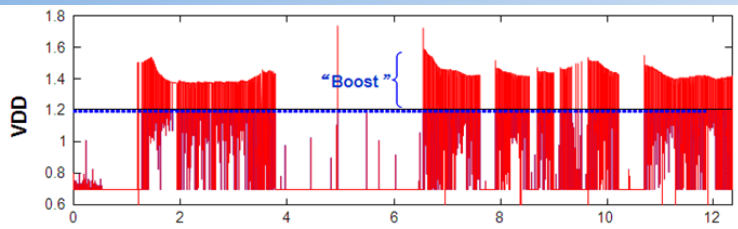
A DRM Framework



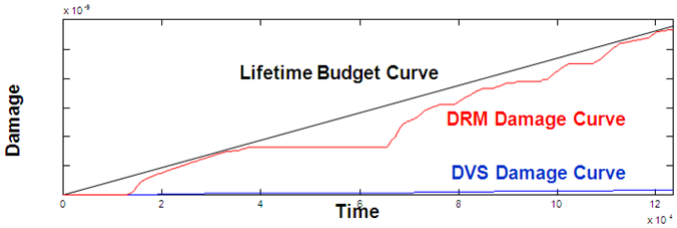
Page ▪ 18

The Impact of Dynamic Reliability Management

DRM voltage control
- Boosts/throttles maximum assignable voltage
- +25% peak performance with typical workload/temperature



In a DRM System, the maximum voltage can be "*boosted*" to allow periods of higher peak performance while maintaining a margin below the budgeted damage curve.



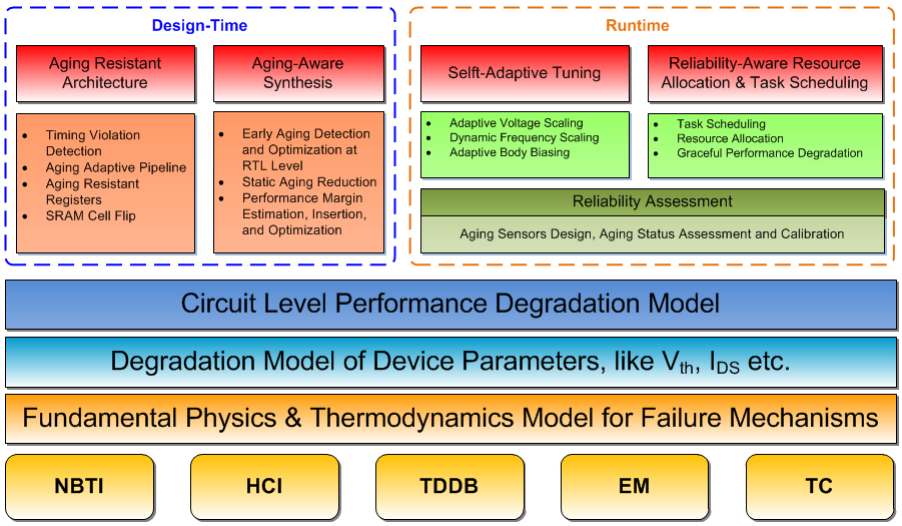
Page ▪ 19

Agenda

1. Introduction
2. Challenges
3. DRM System
4. **DRM Implementation**
5. Conclusion

Page ▪ 20

Reliability-Aware Design and Computing Platforms



Page ▪ 21

DRM System Critical Issues

1 **Degradation Model**

Device degradation model is the corner stone of DRM system, which describes the physical and thermodynamic processes of aging failure mechanisms.

2 **Aging Sensor**

Aging sensors are specific-designed compact circuitries, which are used to online extract the degradation/reliability status from circuit under test/ observation.

3 **Reliability Assessment**

System level reliability status can be obtained by multiple online aging sensors with elaborately selected location, cooperating with certain system level reliability assessment methods.

4 **Reliability Tuning**

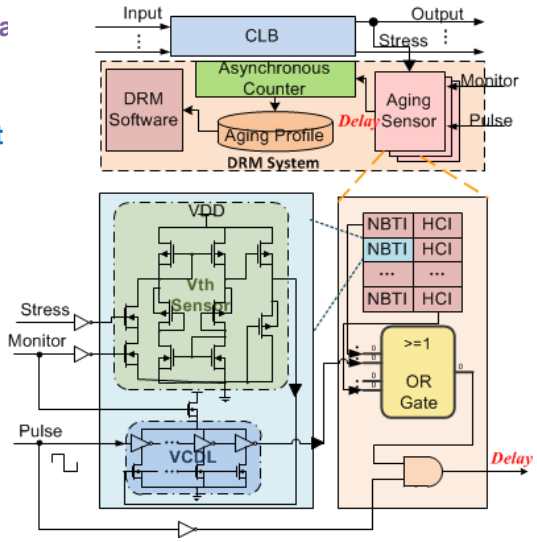
Reliability Tuning techniques include DVFS, task scheduling, body biasing and so on.

Page ▪ 22

DRM Concepts & Aging Sensors

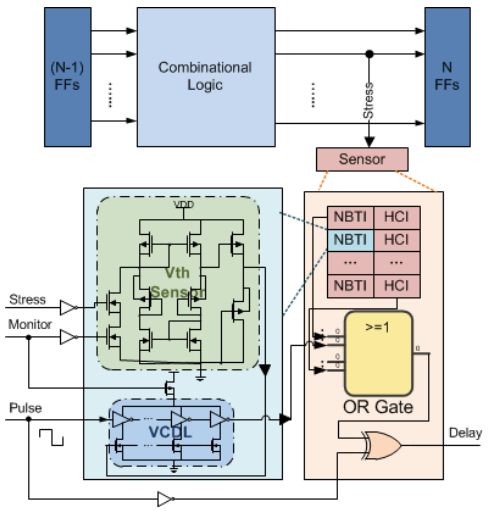
Aging Sensor(s) is the critica component of DRM System

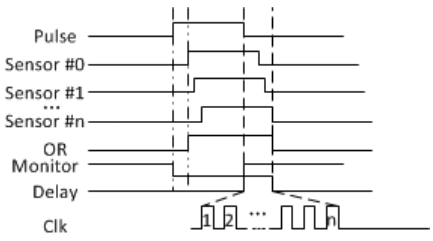
- ***Small*, in-situ deployment**
- ***Non-intrusive* to normal function**
- ***Variation(s)-tolerant***
- **Easy to calibrate**
- **Technology portable**



Page ▪ 23

V_{th}-Based Aging Sensors



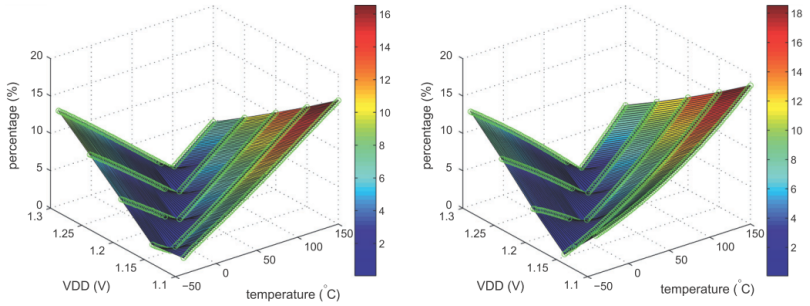


- **Proposed Aging Sensors for NBTI and HCI**
  - ✓ **NBTI, HCI are major reliability concerns of modern ICs**
  - ✓ **V_{th} degrades due to NBTI, HCI**
  - ✓ **Using sacrificed *DUT* to duplicate a same aging stress**
  - ✓ **V_{th} transformed into time-domain using VCDL**

Page ▪ 24

Simulation Results – V&T Stability

V_{th} deviation relative to normal condition (T=27 °C and VDD=1.2 V) with temperature and voltage variations.

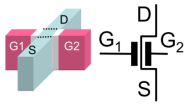


(a) NBTI Sensor (b) HCI Sensor

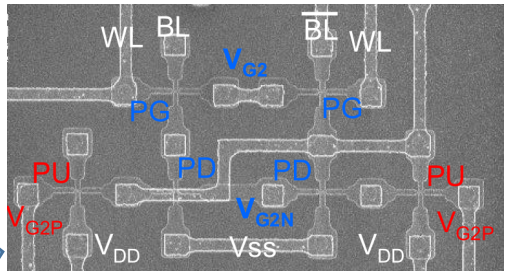
- For extreme conditions (i.e., VDD=1.1V, T=150 °C), the deviation is about 16% for the NBTI sensor, and 17% for the HCI sensor.
- Assume a normal variation range is (0 °C, 60 °C) and VDD±0.05V, the worst case error of the proposed sensors is less than 8%.

IG-FinFET SRAM Cell

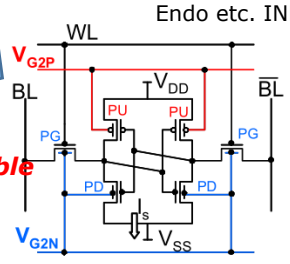
Common-Gate FinFET



Independent-Gate FinFET



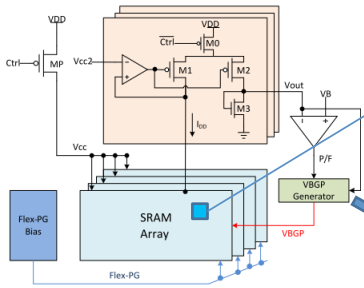
Endo etc. INEC. 2011



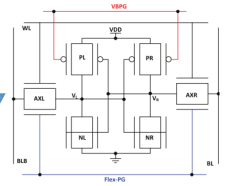
NBTI mitigation is possible by using IG-FinFETs!

IG-FinFET 6T SRAM Cell:
(a) allows to control V_{th} for SRAM cells;
(b) no significant area & power consumption trade-off introduced.

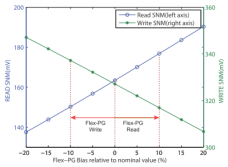
NBTI Mitigation Using I_{DDQ} Monitor



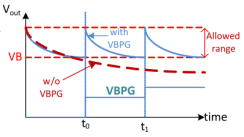
Proposed Mitigation Scheme



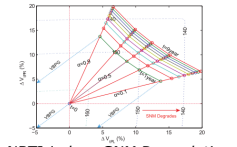
Cell View of Mitigation Scheme



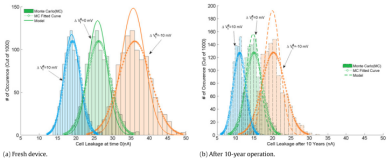
Flex-PG vs. SRAM Read/Write SNM



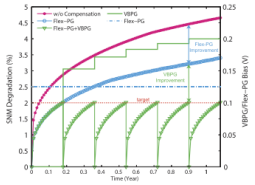
Practical VBPG Compensation



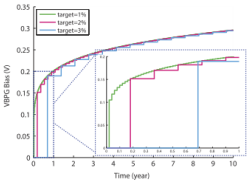
NBTI-induce SNM Degradation



6T-SRAM cell leakage distribution of fresh device and aged device (10-year operation at 50 ° C) using 20 nm FinFET technology with −10 mV, 0 mV, and 10 mV global variations, respectively.

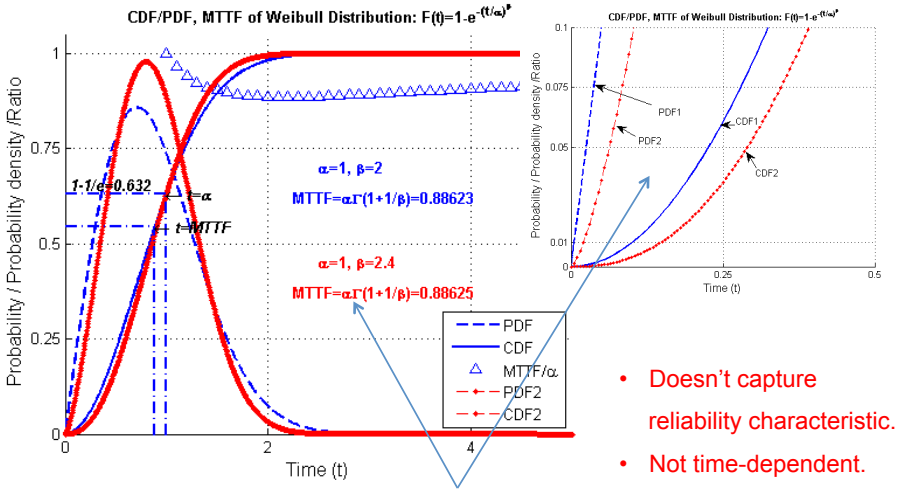


SNM improvement with the VBPG and Flex-PG compensating technique



The applied VBPG bias with different targeted SNM degradation margins.

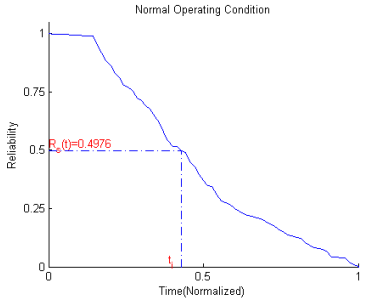
Why Don't We Utilize MTTF?

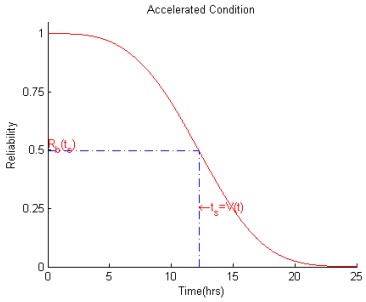


- Doesn't capture reliability characteristic.
- Not time-dependent.

Similar MTTFs, but quite different reliability characteristic during operating time

Virtual Age Model





Virtual age can be defined as the **equivalent reliability status** in a stochastic working environment when referring to a baseline environment.

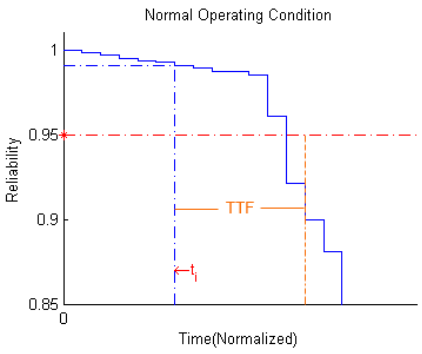
$$R_s(t) = R_b(t_s)$$

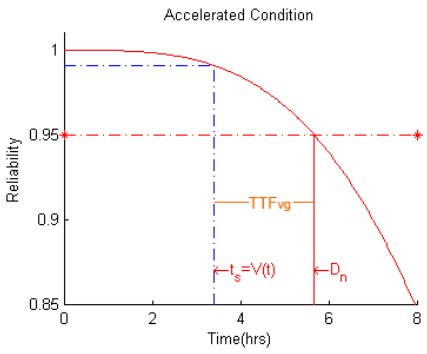
Virtual age can be computed as:

$$t_s = V(t) = R_b^{-1}(R_s(t))$$

Page ▪ 29

Time-to-Failure (TTF)





IC's expected operational life can be defined as:

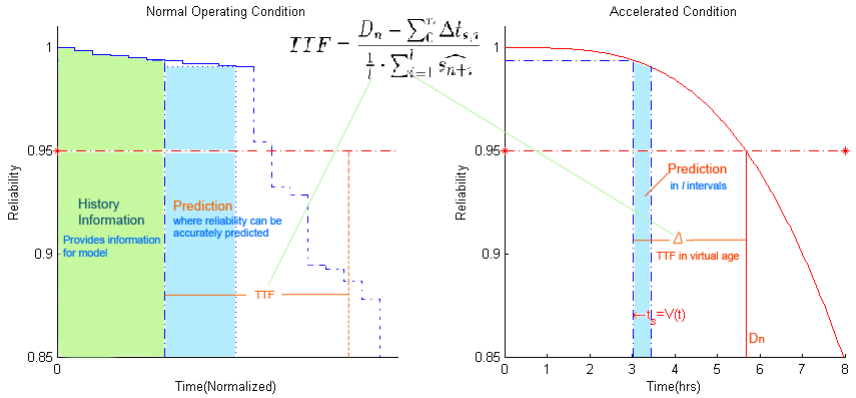
$$D_n = TTF(n) = R_b^{-1}(1-n)$$

Thus equivalent virtual age of TTF is:

$$TTF^n = TTF(n) - VirtualAge = R_b^{-1}(1-n) - \sum_0^n \Delta t_{s,i}$$

Page ▪ 30

TTF Estimation



By using double exponential smoothing, TTF can be estimated as:

$$TTF = \frac{D_n - \sum_0^n \Delta t_{s,i}}{\frac{1}{l} \cdot \sum_{i=1}^{l} \widehat{s_{n+i}}}$$

where $\widehat{s_{n+i}}$ is the estimated "aging" speed of next *l* intervals.

Page ▪ 31

Conclusions

- Reliability situation is severer than ever in IC designs, and it's getting worse and worse;
- DRM handles gradual reliability threats at run-time; DRM is not only important for safety-critical applications, but also for consumer electronics in daily life;
- Multi-/Many-core processors provide a great opportunity to perform DRM on these platforms;
- PVT variations must be considered in order to have an accurate measurement from on-chip aging sensors.

Page ▪ 32

Related Publications

- Y. Wang, S. D. Cotofana, L. Fang, Analysis of the Impact of Spatial and Temporal Variation on the Stability of SRAM Arrays and Mitigation Technique Using Independent-Gate Devices, *JPDC*, 2013
- N. Cucu Laurenciu, S.D. Cotofana, A Nonlinear Degradation Path Dependent End-of-Life Estimation Framework from Noisy Observations, *Microelectronics Reliability*, 2013
- N. Cucu Laurenciu, Y. Wang, S. D. Cotofana, A Direct Measurement Scheme of Amalgamated Aging Effects with Novel On-Chip Sensor, *VLSI-SoC*, 2013
- N. Cucu Laurenciu, S.D. Cotofana, Critical Transistors Nexus Based Circuit-Level Aging Assessment and Prediction, *JPDC,* 2013
- Y. Wang, S. D. Cotofana, L. Fang, Lifetime Reliability Assessment with Aging Information from Low-Level Sensors, *GLSVLSI*, 201
- Y. Wang, M. Enachescu, S. D. Cotofana, L. Fang, Variation Tolerant On-Chip Degradation Sensors for Dynamic Reliability Management Systems, *Microelectronics Reliability*, 2012
- N. Cucu Laurenciu, S.D. Cotofana, Context Aware Slope Based Transistor-Level Aging Model, *Microelectronics Reliability*, 2012
- N. Cucu Laurenciu, S.D. Cotofana, A Markovian, Variation-Aware Circuit-Level Aging Model, *NANOARCH,* 2012
- Y. Wang, S. D. Cotofana, L. Fang, Statistical Reliability Analysis of NBTI Impact on FinFET SRAMs and Mitigation Technique Using Independent-Gate Devices, *NANOARCH*, 2012
- Y. Wang, S. D. Cotofana, L. Fang, A Unified Aging Model of NBTI and HCI Degradation towards Lifetime Reliability Management for Nanoscale MOSFET Circuits, *NANOARCH*, 2011
- Y. Wang, S. D. Cotofana, L. Fang, A Novel Virtual Age Reliability Model for Time-to-Failure Prediction, *IIRW*, 2010