Low Power Multicore SoC Architecture for UWB MAC Processing

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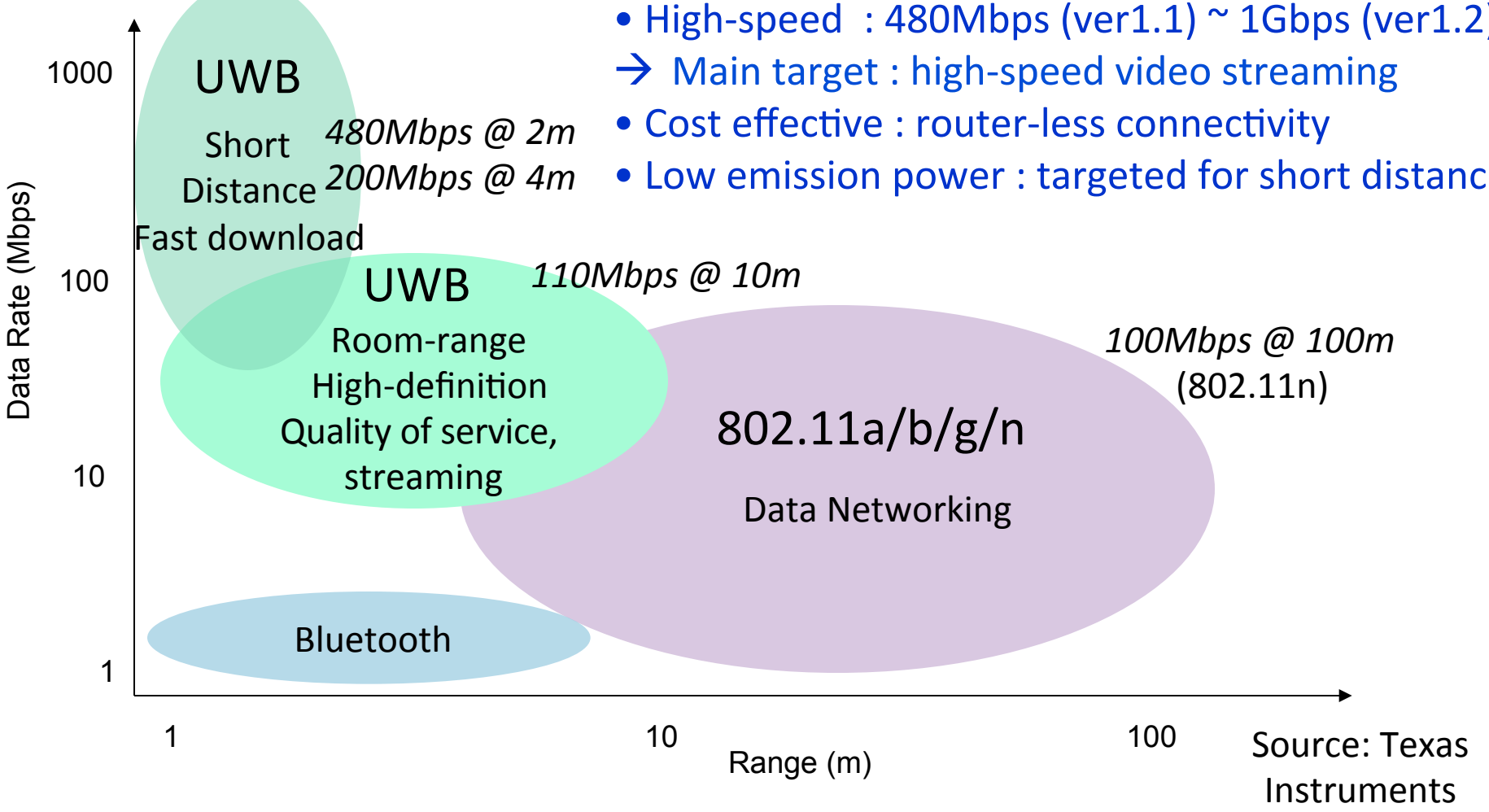
UWB Technology

Wireless personal area networking (WPAN)

- High-speed : 480Mbps (ver1.1) ~ 1Gbps (ver1.2)

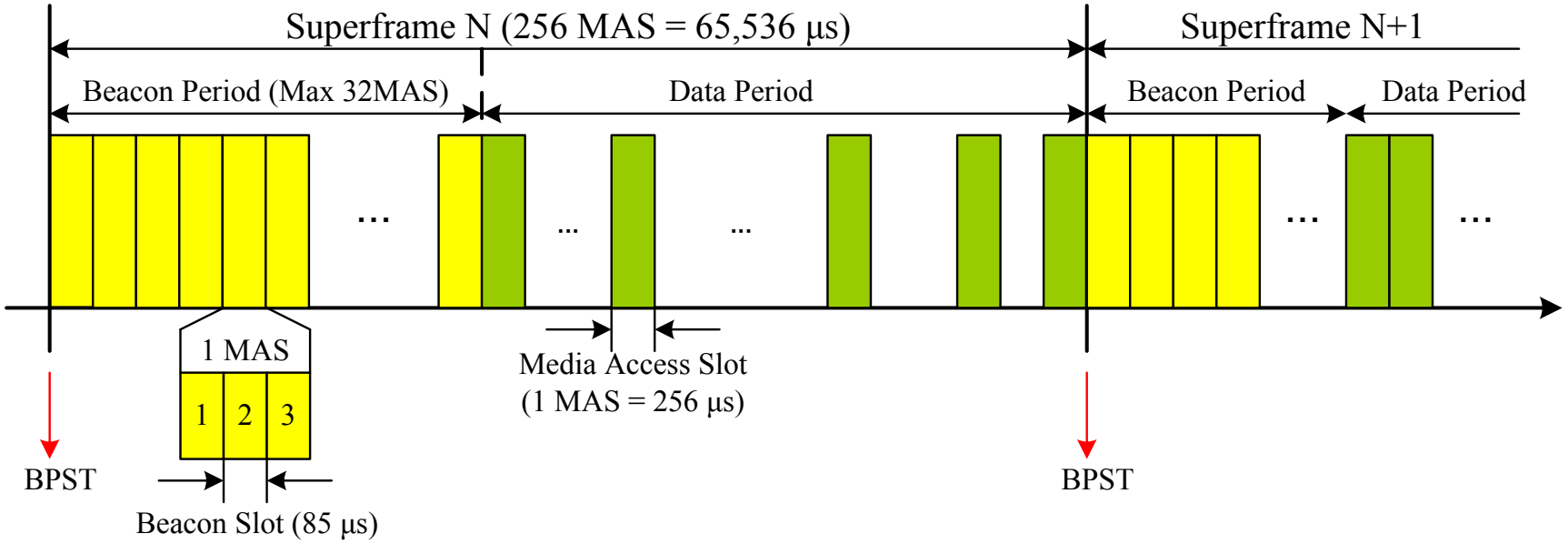
→ Main target : high-speed video streaming

- Cost effective : router-less connectivity
- Low emission power : targeted for short distance



Source: Texas Instruments

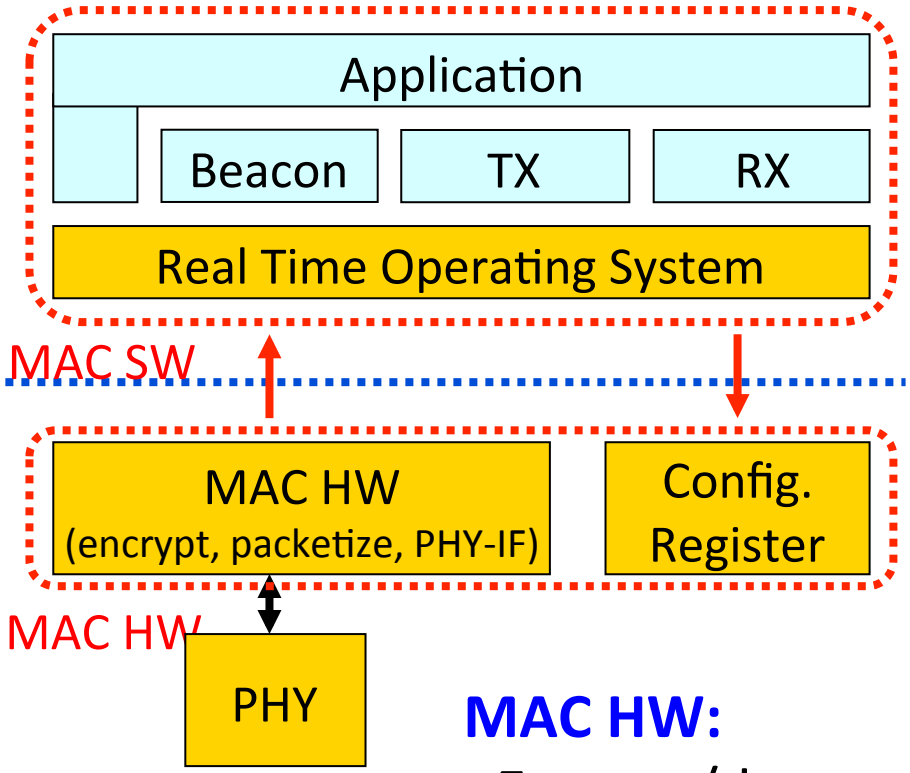
WiMedia UWB MAC Protocol



- TDMA (time-division multiple access) : Priority-based and reservation-based QoS guarantee
- Fully distributed (router-less) network: all UWB terminals exchange network status information during “Beacon Period” to negotiate bandwidth demands

→ Very tight timing budget (finely controlled by RTOS)

UWB MAC SW/HW Architecture



Multi-tasked SW modules

- Main (Appl): payload processing
- Beacon: network scheduling
- TX: payload transfer
- RX: payload receive

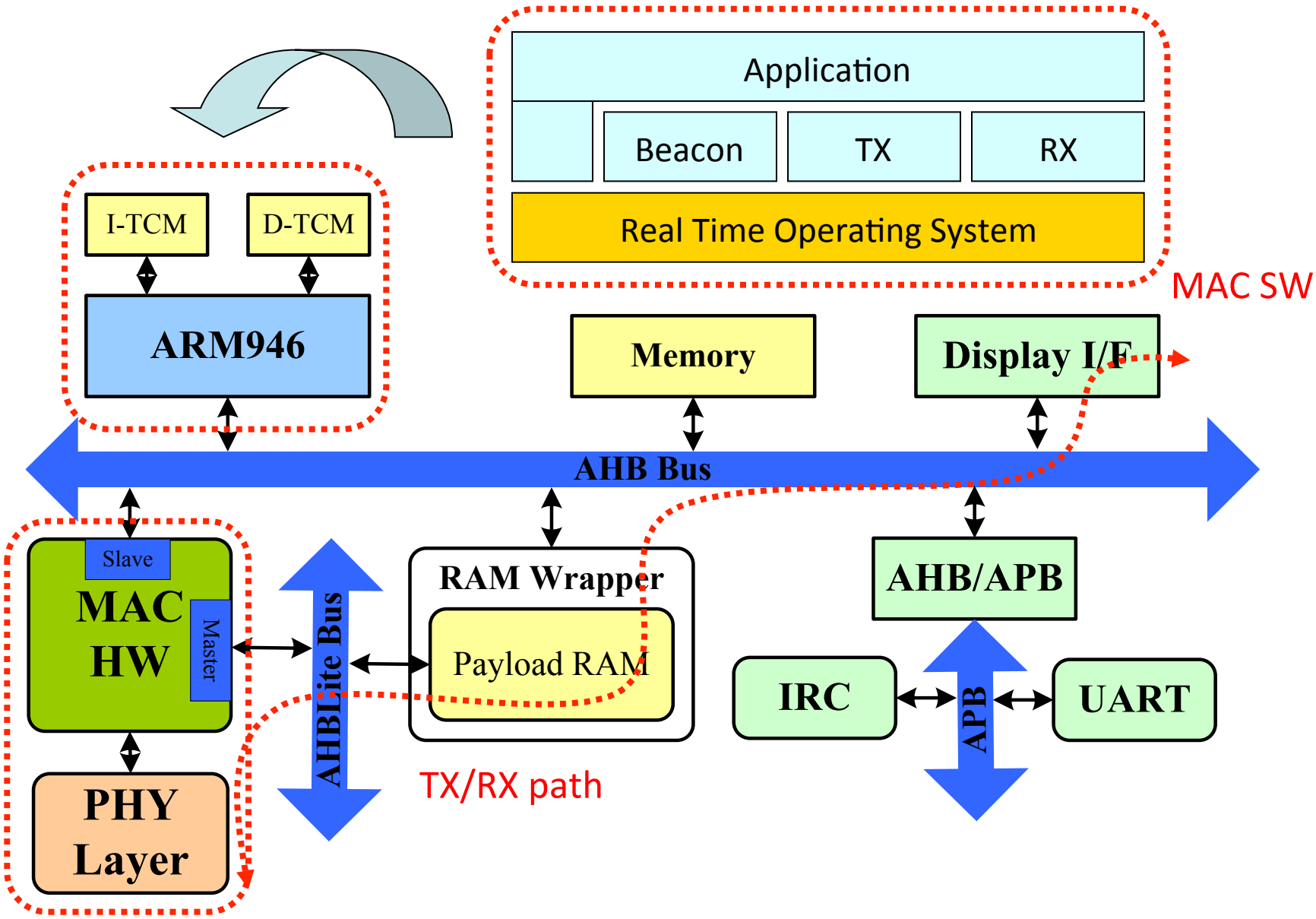
RTOS services

- Task switching/scheduling
- Inter-task messaging/sync.
- HW Interrupt handlers

MAC HW:

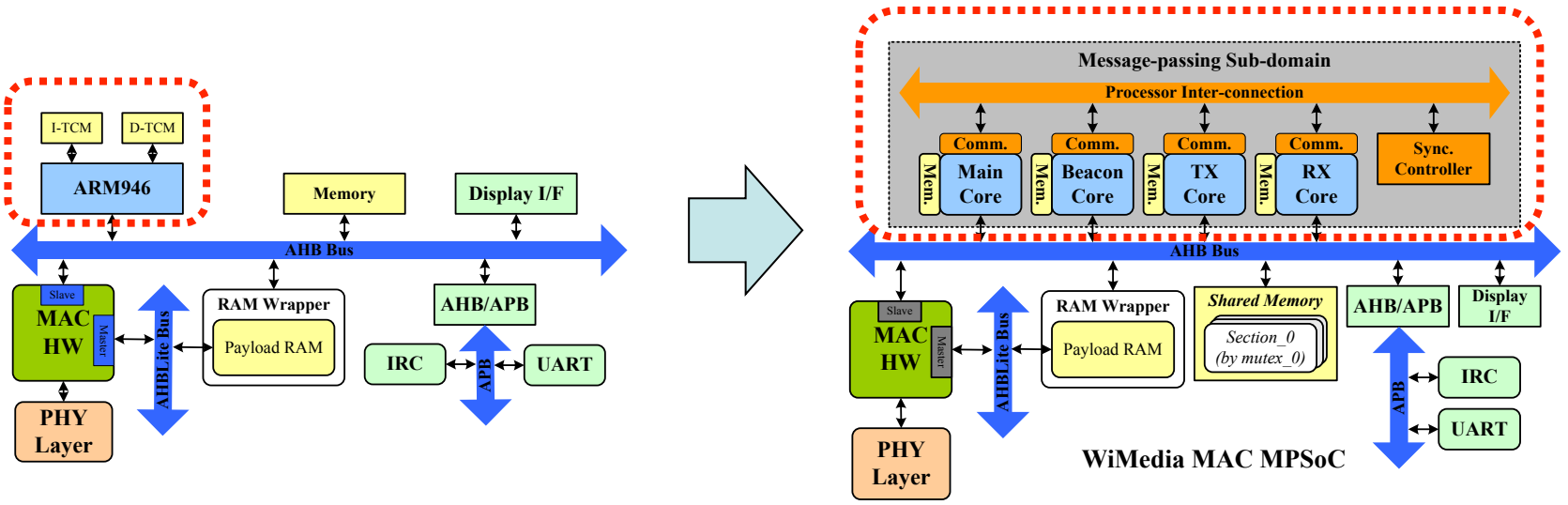
- Encrypt/decrypt
- Payload packetize/de-packetize
- PHY-IF: payload FIFO interface

Single-CPU Architecture



Design Goals

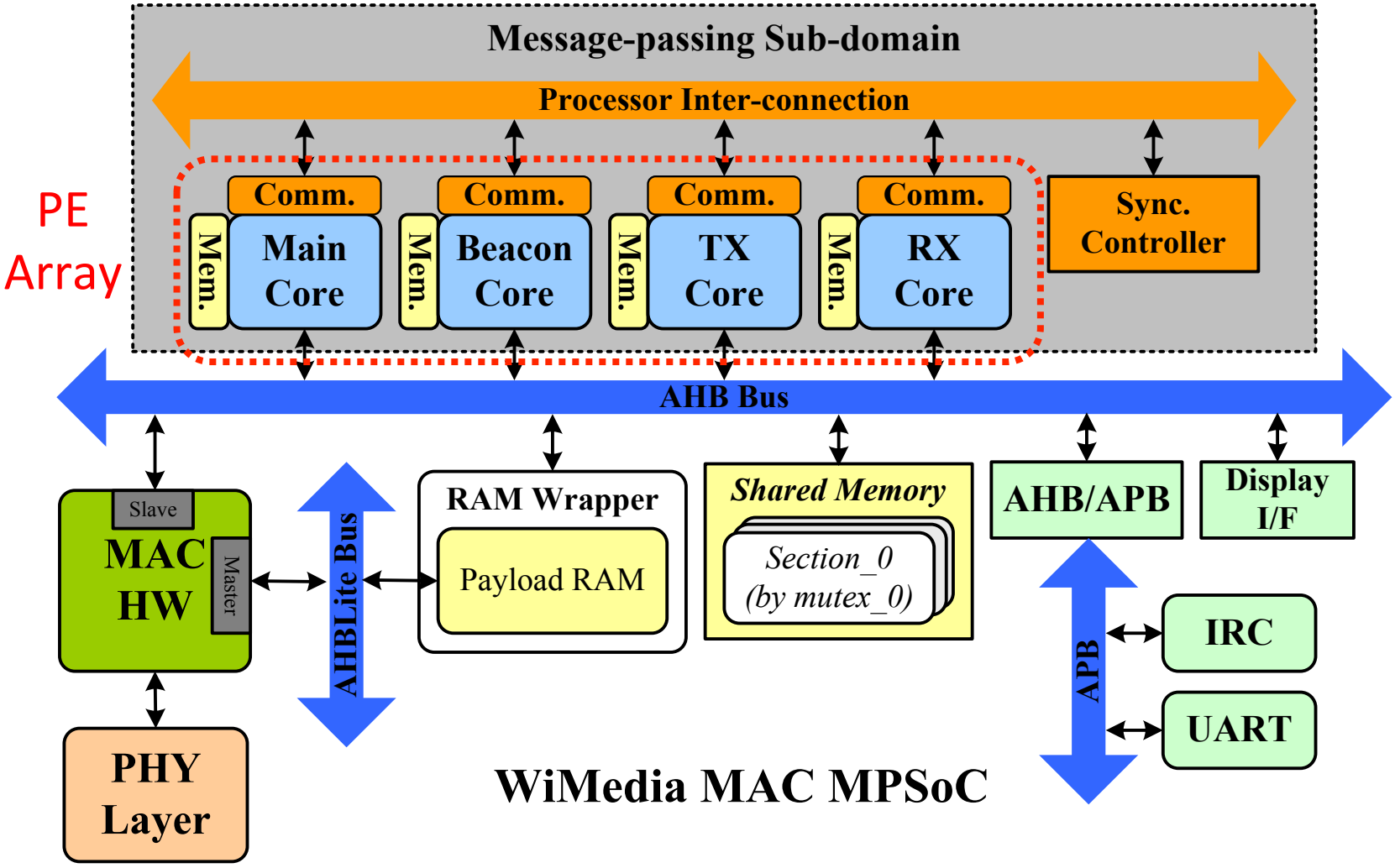
- Decrease SW workloads via multi-core
  - One core per task → 4 cores (Main/Beacon/TX/RX)
  - Eliminate RTOS overhead → efficient inter-core messaging and synchronization infrastructure
  - Power-efficient processor cores with built-in messaging and synchronization capabilities



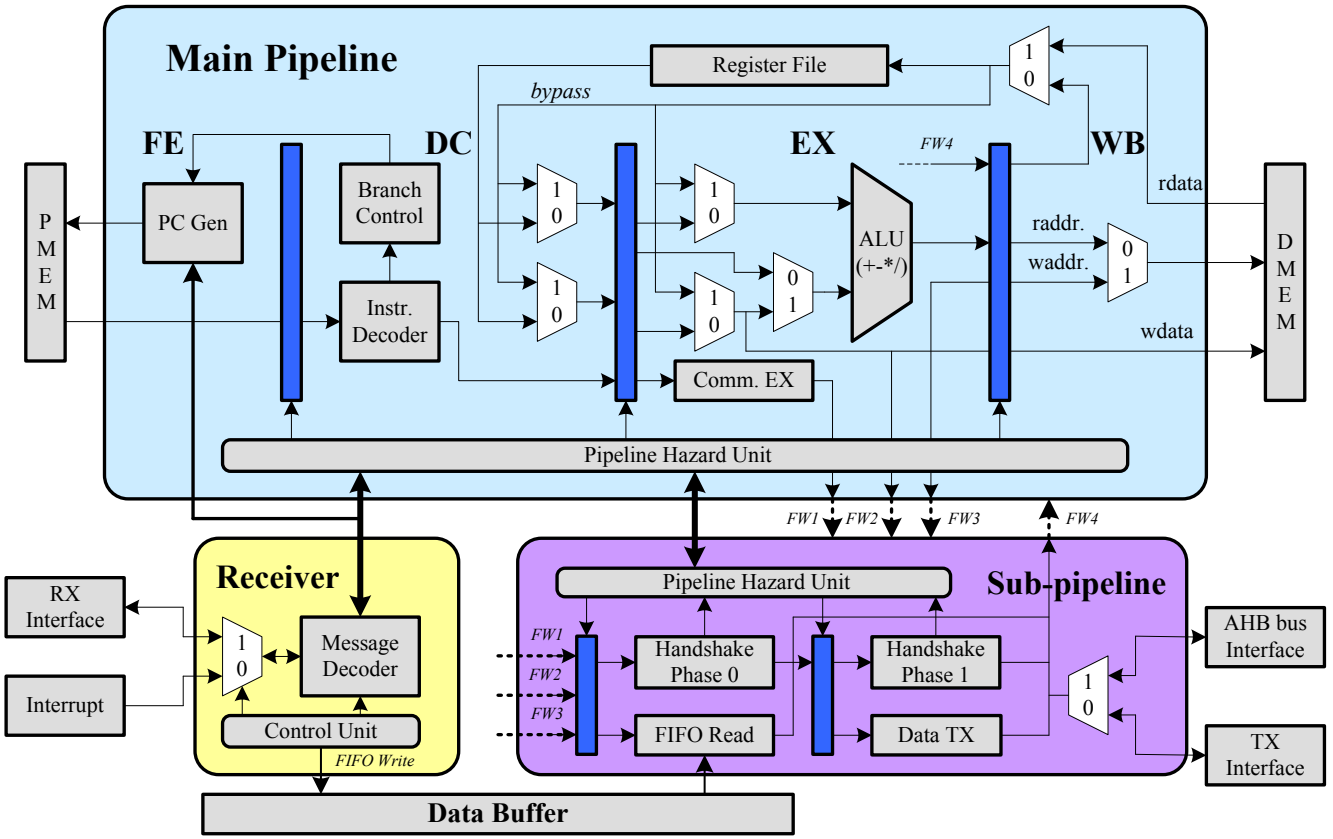
Design Migration Steps

- Maximize reuse of existing single-core SW codes
  - Minimal changes to task codes for SW maintenance
  - SW wrappers to RTOS kernel APIs → replace inter-task messaging/sync with inter-core messaging/sync
  - Use the same core (ARM946) for all cores → reuse SW development environment
- Processor core optimization
  - Dedicated simple RISC core with messaging and synchronization capabilities
  - Dedicated inter-core interconnect with synchronization controller for efficient inter-core “locks” and messaging

Proposed MPSoC Architecture



Processor Architecture (TCT-Proc)

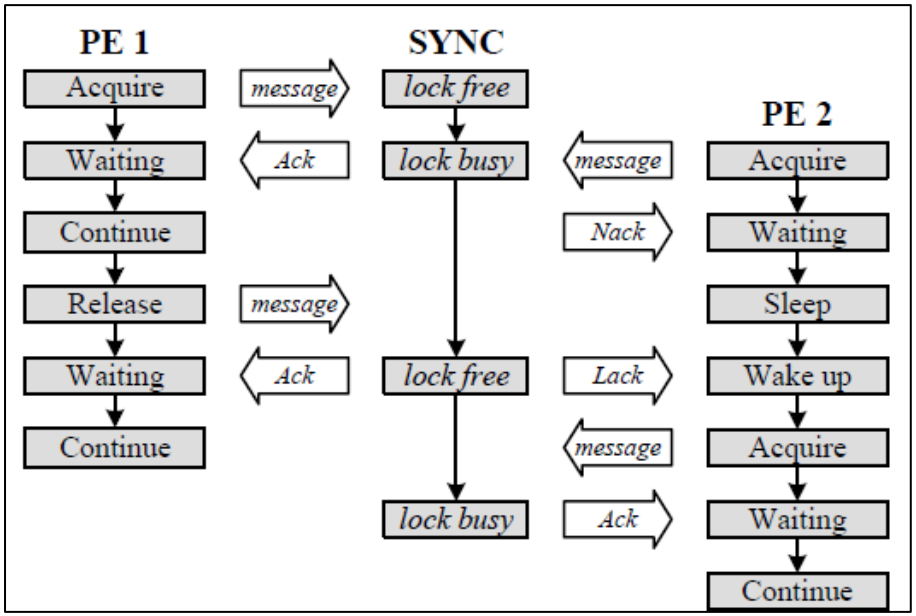


Technology	Main core	Comm.	AHB I/F	Total Gate
90nm	31,049	3,354	5,089	39,493

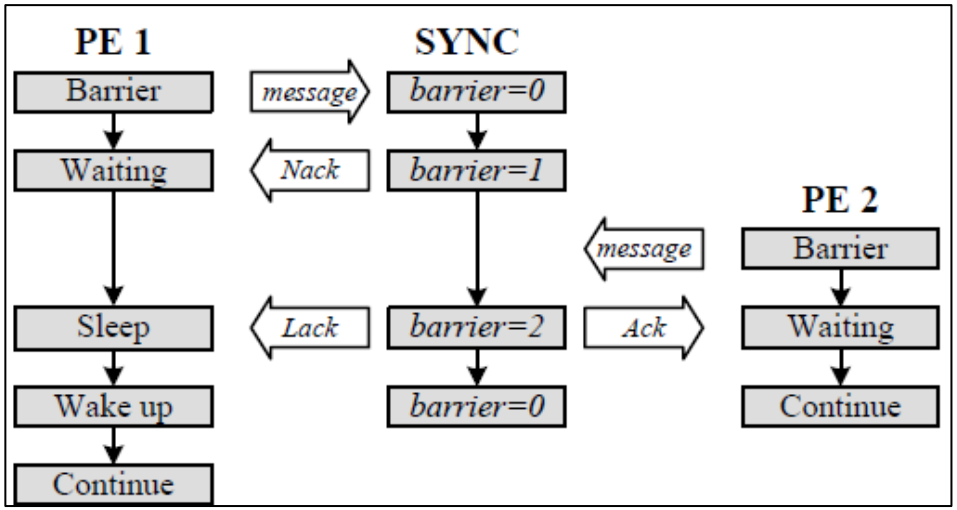
* Designed on Synopsys Processor Designer

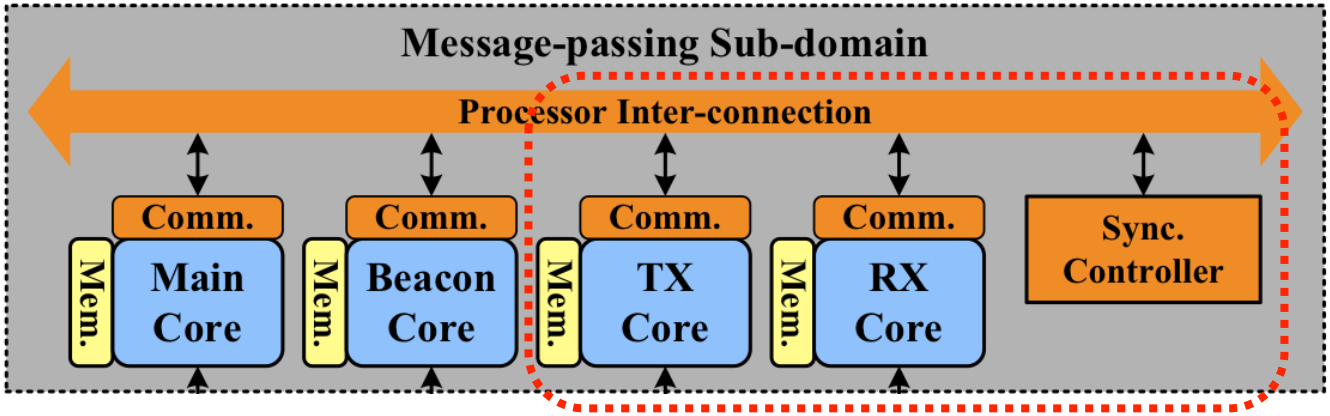
Inter-Core Synchronizer

LOCK

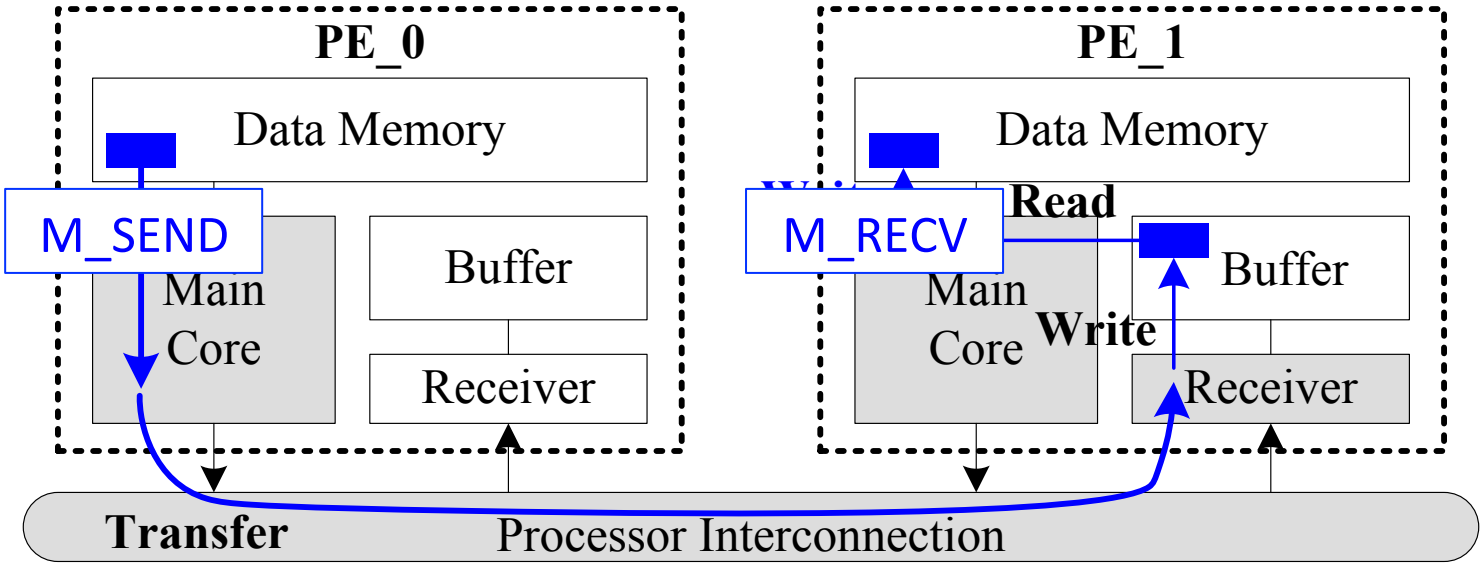


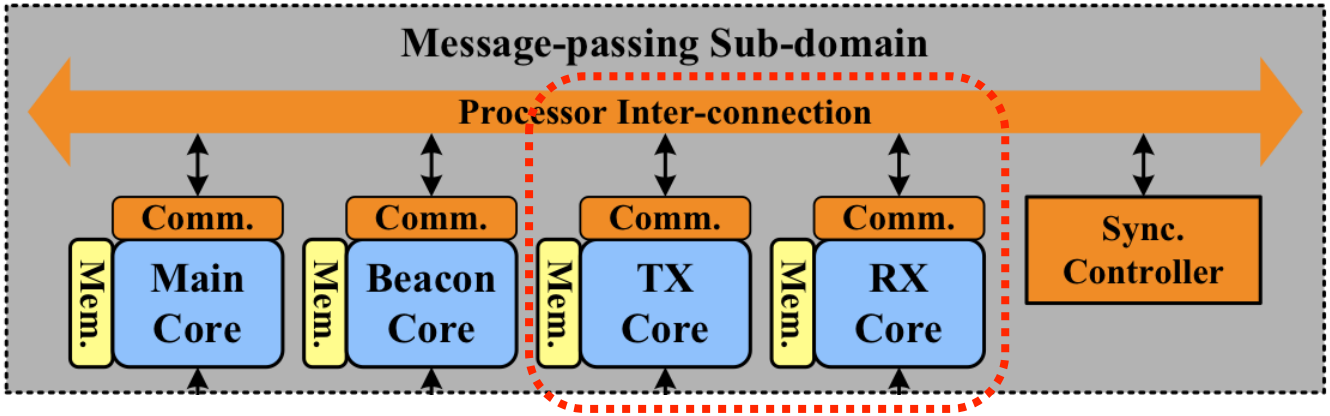
BARRIER





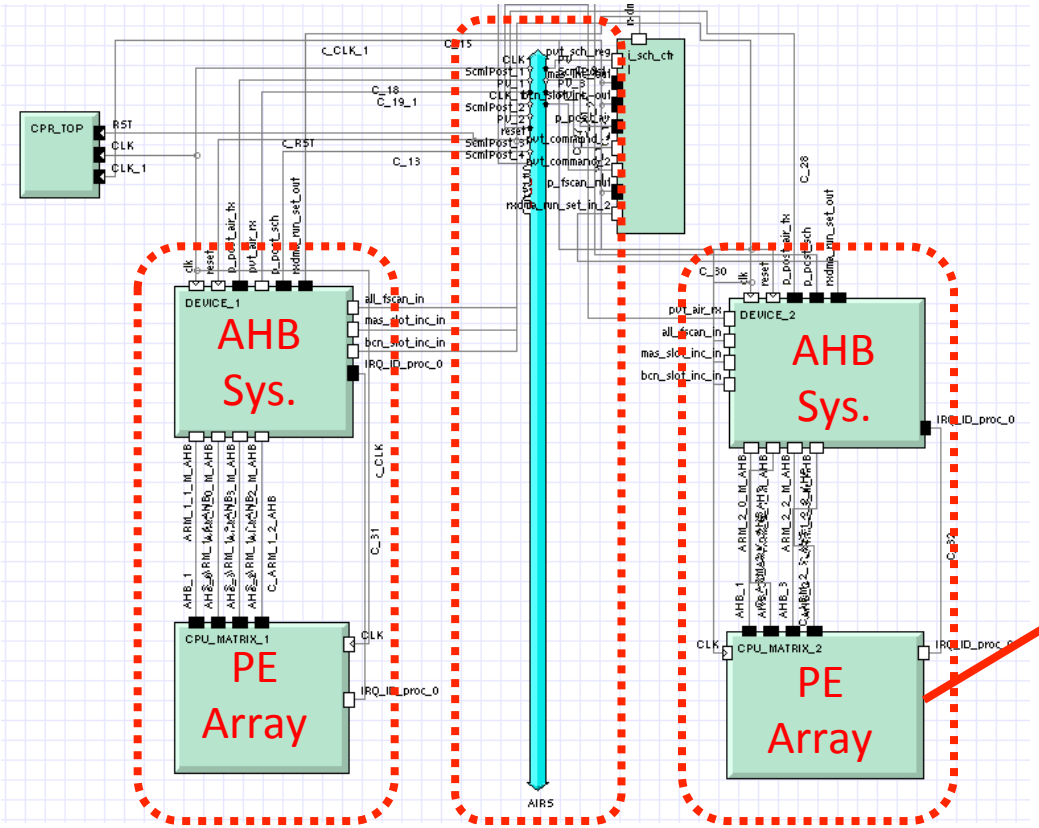
Inter-Core Data Transfer

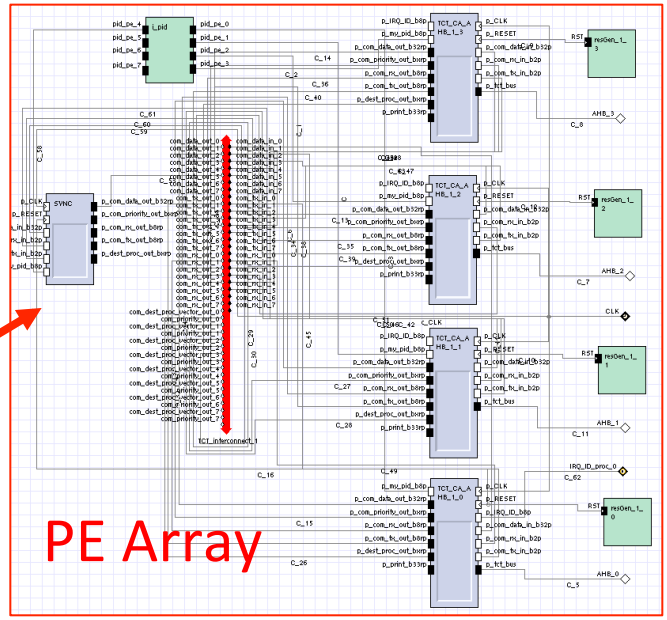




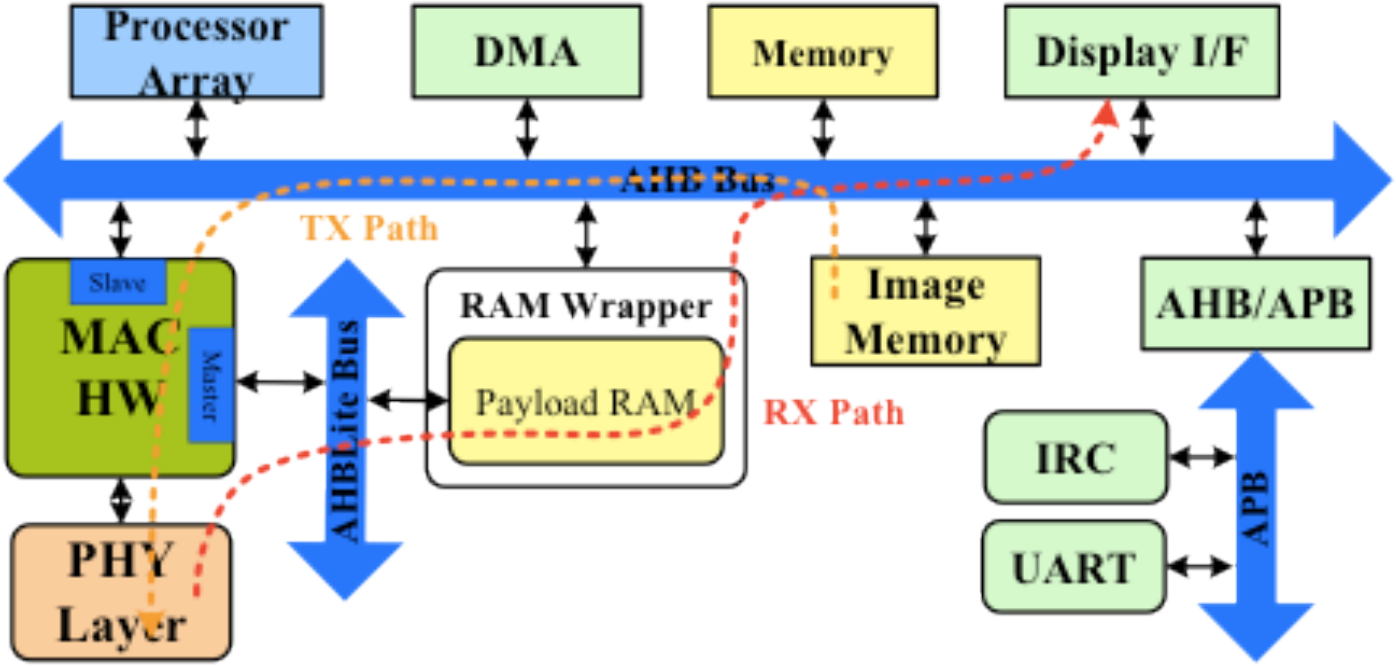
System Simulation Setup

System Modeling on Synopsys Platform Architect



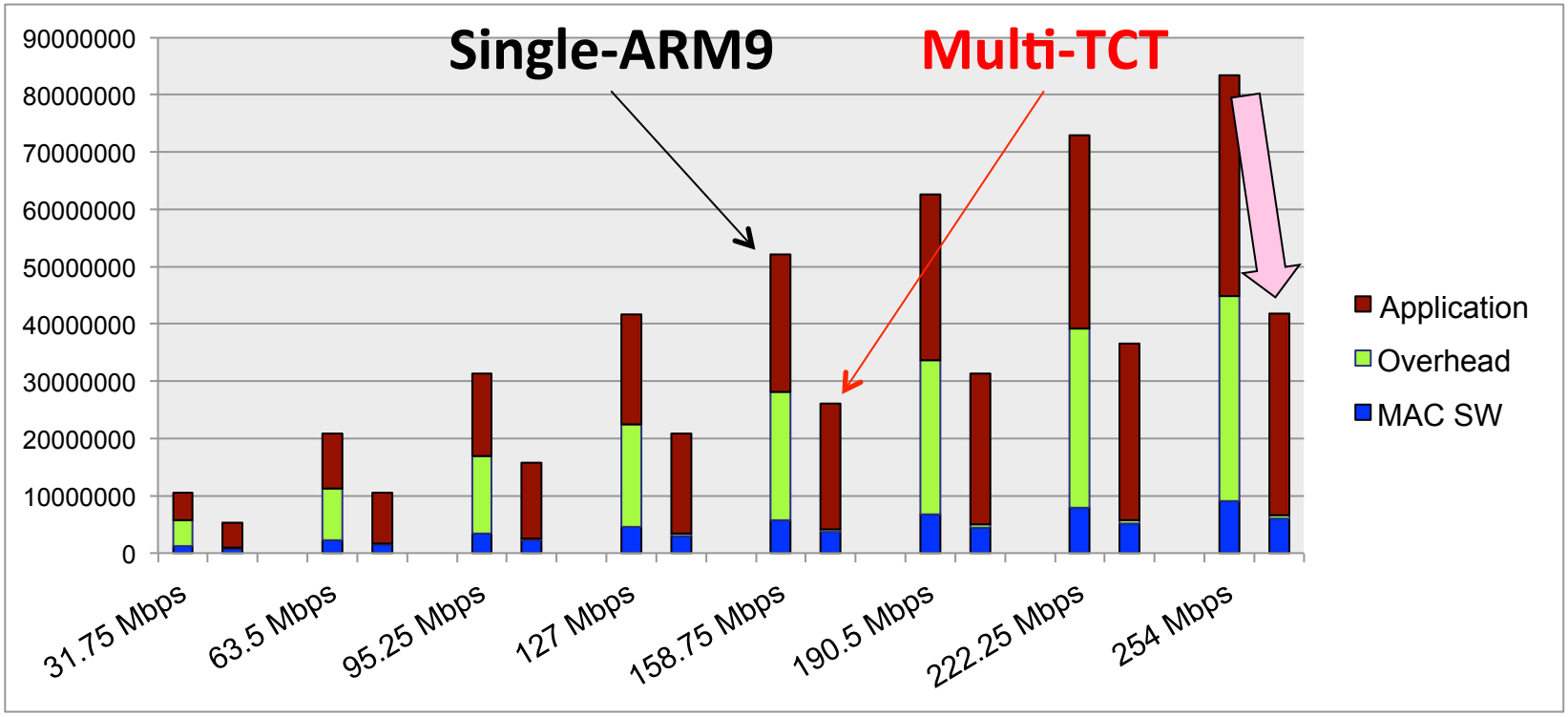


Simulation Scenario



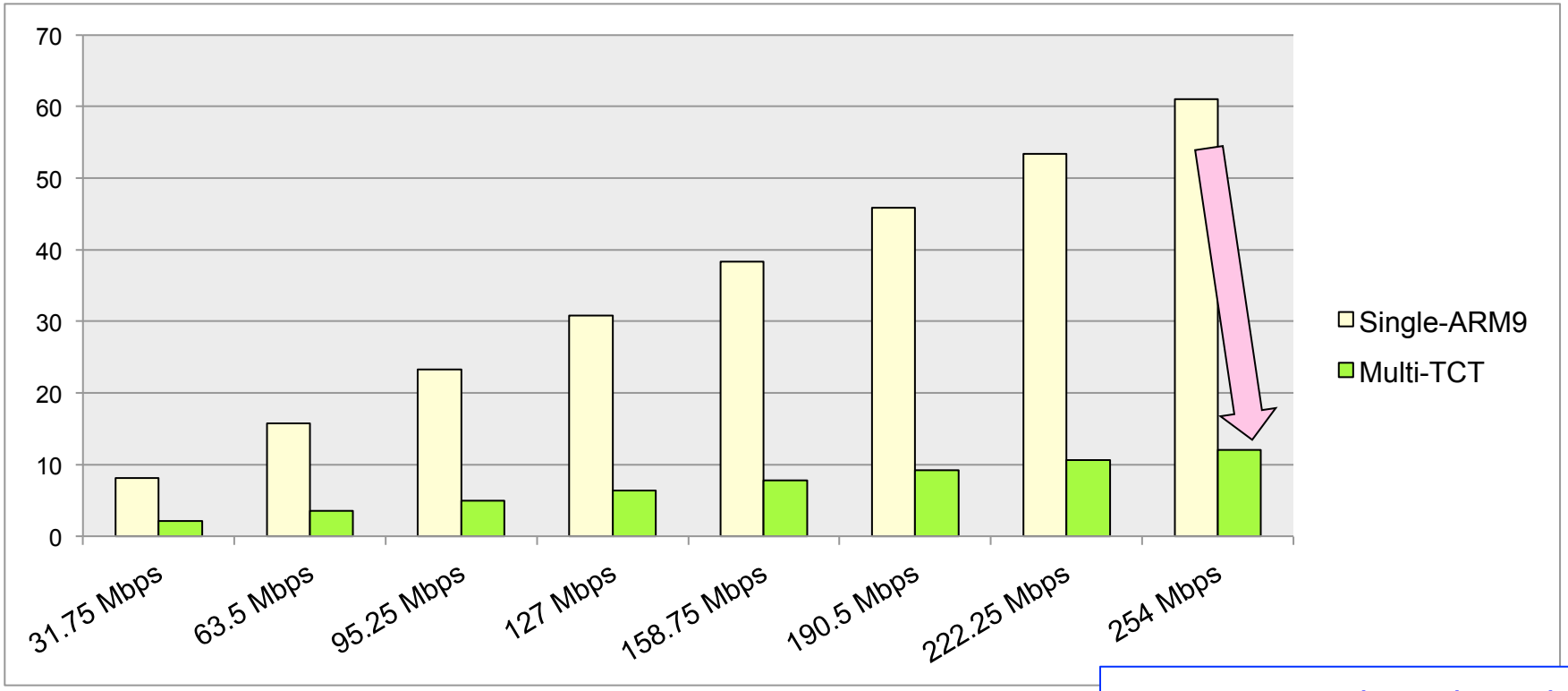
- TX path : Read image data from memory and transmit as payloads
- RX path : receive payloads and send to display device
- # frames per MAS (Media Access Slot) : 1 ~ 8 (31.8Mbps ~ 254Mbps)

SW Workload Breakdown



- Significant "Overhead" reduction
  - Task switching/scheduling : eliminated by core-per-task
  - Locks, barriers, messaging : accelerated by Sync. Controller
- Total cycle count reduction : **1.99x**

Power Consumption



- Power reduction : **3.83x ~ 5.00x**
- Area comparison @ 90nm CMOS
  - ARM946E-S (w/o cache): 0.303 mm^2
  - TCT-proc x 4 + SYNC-controller: 0.414 mm^2

Running each task with smaller core (~1/3 area) results in higher power efficiency

Summary

- **UWB MAC processing:**
  - Tight timing budget managed on multi-task/RTOS on single-core architecture → large overhead in RTOS services (task switching/scheduling, synchronization, messaging)
- **Multi-core architecture for UWB MAC:**
  - One core → one task : eliminate task switching overhead
  - Large portion of multi-task SW reusable with API wrappers
  - Fast synchronization & messaging capabilities in each core
  - Cycle count reduction: **1.99x** → task switching overhead elimination
  - Power reduction: **5.00x** → tasks running on small cores

Thank You for Your Attention!

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