

SYNOPSYS® Silicon to Software

















Monday July 03: Enabling Technologies For MPSoC

08:00 Registration continued

Session 1: Keynote

08:30 Giovanni De Micheli, EPFL, Switzerland,Emerging Technologies For Computing09:30 Break

Session 2 : Mini-Keynote Presentations

- **10:00** Jishen Zhao, UCSC, USA, **Transaction Cache:** *A Persistent Memory Acceleration* **Approach**
- 10:12 Wei Zhang, Hong Kong University of Science and Technology, Hong Kong, Exploration of Cache Coherence for CPU FPGA Heterogeneous System
- 10:24 Tohru Ishihara, Kyoto Univ., Japan, *Minimum Energy Point Tracking for Self Powered* IoT Processors
- 10:36 Youn-Long Lin, National Tsing Hua University, Taiwan, Multi-Core and GPGPU Acceleration of Video Coding
- 10:48 Yoshinori Takeuchi, Osaka University, Japan, Reliable multiprocessor system for low voltage MPSoC
- 11:00 Masaaki Kondo, Tokyo Univ., Japan, Energy Efficient Network-on-Chips with Opportunistic Circuit-Switching for MPSoCs
- 11:12 Ittetsu Taniguchi, Ritsumeikan University,
 Japan, An Autonomous Decentralized Mechanism for
 Energy Interchanges with Accelerated Diffusion
 Based on MCMC
- 11:24 Panel discussion with the lecturers
- 12:30 Lunch

Session 3: In-Depth Presentations

14:00 Doris Keitel-Schulz, Infineon, Germany, *IoT –the world of connected devices*

Session 3: In-Depth Presentations

- 14:30 Marcello Coppola, STMicroelectronics, France, *Making Driving More Connected and More Secure*
- 15:00 Akihiko Shinya, NTT Nanophotonics Center, Japan, Nanophotonics for low-latency optical integrated circuits
- 15:30 Break

Session 4: In-Depth Presentations

- 16:00 Hironori Kasahara, Waseda University, Japan, Automatic Cache and Local Memory Optimization for Multicores
- 16:30 Yuichi Nakamura, NEC Corp., Japan, From Software Defined Network (SDN) to Software Defined Infrastructure (SDI)
- 17:00 Pieter Van Der Wolf, Synopsys, The Netherlands, *Processor Solutions for Energy-Efficient IoT Applications*
- 17:30 Panel discussion with the lecturers
- **20:00** Dinner

Tuesday July 04: High Performance Computing

Session 5: Keynote

08:30 Pankaj Mehra, Western Digital Corporation,USA, *Data-Centric Computer Architecture*09:30 Break

Session 6 : Mini-Keynote Presentations

- **10:00** Yoshifumi Sakamoto, IBM, Japan, *Neuromophic device for Automotive*
- 10:12 Yuko Hara-Azumi, Tokyo Institute of Technology, Japan, Energy-Efficient Multicore Processor For Large Stream Data In IOT Systems

- 10:24 Kees van Berkel, Eindhoven University of Technology, The Netherlands, Exascale Computing for Radio Astronomy. How to program?
- 10:36 Koji Inoue, Kyushu University, Japan,
 Predictive Sensing and Adaptive Management For
 RealTime Applications
- **10:48** Sungjoo Yoo, Seoul National University, Korea, ZeNA: Zero-Aware Neural Network Accelerator
- 11:00 Norbert Wehn, University of Kaiserslautern, Germany, DRAM Memory Controller From General Application Specific Architectures
- 11:12 Masaki Gondo, eSOL Co. Ltd., Japan,
 Introduction to AUTOSAR Adaptive Platform and
 an Approach to high-performance computing
- 11:24 Panel discussion with the lecturers

Session 7: In-Depth Presentations

- 14:00 K. Charles Janac, Arteris Inc., USA, Resilient Interconnect for Functionally Safe Automotive SoCs
- **14:30** Benoît de Dinechin, Kalray, France, Supporting Standard CNN inference on manycore processors
- **15:00** Eric Monchalin, ATOS, France, *Extreme Computing, strategic directions for the 2020s*

Session 8: In-Depth Presentations/Contest

- **16:00** Victor Grimblatt, Synopsys, Chile, *MPSoC* Latin America Contest 2017
- **16:05** Javier Carvajal, ImagineXYZ, Costa Rica, *Remora: Bringing back balance to the ocean*
- 16:20 Takashi Miyamori, Toshiba Corporation, Japan, Efficient Implementations of Deep Neural Network Hardware
- 16:50 John Goodacre, University of Manchester/Kaleao Ltd/ARM Ltd, UK, Should the semiconductor industry embrace silicon modularity?
- **17:20** Panel discussion with the lecturers
- **18:30** Boat Tour
- **20:30** Dinner

Wednesday July 05: Embedded Computing

Session 9 : Keynote

08:30 Ivo Bolsens, Xilinx, USA, Unleashing the full performance of the All Programmable FPGA while abstracting the hardware details
 09:30 Break

Session 10: Mini-Keynote Presentations

- 10:00 Rolf Ernst, Technische Universität
 Braunschweig, Germany, Effects of Dynamic NoC
 Resource Management for Mixed Criticality
 Applications
- 10:12 Jiang Xu, Hong Kong University of Science and Technology, Hong Kong, *Break Memory Wall Through Silicon Photonics*
- 10:24 Frederic Rousseau, TIMA, France, Accurate Study and Optimization of Synchronization Barriers in a NoC Based MPSoC Architecture
- **10:36** Fabien Clermidy, CEA-Leti, France, *Photonic MPSoC*
- **10:48** Weihua Sheng, Silexica, Germany, *Multicore Use Cases in Automotive*
- 11:00 Hiroki Matsutani, Keio University, Japan, Accelerator Design for Big Data Processing Frameworks
- 11:12 Shinya Takamaeda, Hokkaido University, Japan, Energy-Efficient In-Memory Neural Network Processor
- 11:24 Panel discussion with the lecturers
- 12:30 Lunch

Session 11: In-Depth Presentations

- **14:00** Julian Chesterfield, OnApp, UK,
- **14:30** Ran Ginosar, Technion-Israel Institute of Technology, Israël, *Shared Memory Manycore with Hardware Scheduling*
- 15:00 Gabriela Nicolescu, Ecole Polytechnique de Montréal, Canada, *Data Stream Clustering for IoT*15:30 Break

Session 12: In-Depth Presentations

- **16:00** Arnaud Grasset, Thales Research Tech., France, *Designing Efficient and Dependable embedded systems for critical applications*
- 16:30 Masahiko Yoshimoto, Kobe University, Japan, A Wearable Biomedical Sensing System with Normally-off Computing Architecture
- 17:00 Hiroyuki Komori, Socionext, Inc., Japan, Adhocracy Innovation with Imaging technology
- 17:30 Panel discussion with the lecturers
- **18:30** Speakers Meeting
- 20:00 Gala Dinner

Thursday July 06: Automotive

Session 13: Keynote

08:30 Hans-Joerg Voegel, BMW, Germany,Driving and Being Driven: Thoughts on FutureMobility and Technological Drivers

09:30 Break

Session 14: Mini-Keynote Presentations

10:00 Rui Hou, Chinese Academy of Sciences, China, RAGuard: *A Hardware Based Mechanism* for Backward-Edge Control Flow Integrity

10:12 Marilyn Wolf, Georgia Tech, USA, SystemLevel Thermal Modeling and Optimization

10:24 Fumio Arakawa, Nagoya University, Japan, *Cipher IP for IoT Devices*

10:36 Anca Molnos, CEA-Leti, France,

AccuracyEnergy Trade-off with Dynamic

Adequate Operators Using Run-Time Back Bias

10:48 Tsuyoshi Isshiki, Tokyo Institute of Technology, Japan, C++ Object-Oriented RTL Modeling for System-Level Synthesis/Verification on the C2RTL Framework

11:00 Koichiro Yamashita, Fujitsu Laboratories LTD., Japan, An Architecture Design for Integrated Traffic Control System

11:12 Yoshihiko Hirota/Masahiro Murakami, Konica Minolta, Japan, *Designing Structure of Image Processing in MFP*

11:24 Panel discussion with the lecturers

12:30 Lunch

Session 15: In-Depth Presentations

14:00 Andreas Herkersdorf, TU Munich, Germany, Information Processing Factory – Conquering MPSoC Complexity with Self-Aware Computing Platforms

14:30 Yankin Tanurhan, Synopsys, USA,

Designing Scalable Multi Processor Embedded

Vision Solutions

15:00 Kees Vissers, Xilinx, USA, A Framework for Reduced Precision Neural Networks on FPGAs15:30 Break

Session 16: In-Depth Presentations

16:00 Rocco Jonack, NetSpeed Systems, USA, Machine Learning Based Intelligent Interconnect for Next Generation Autonomous Vehicle SoCs **16:30** Tsuyoshi Sato, Pioneer, Japan, *Technology* for Highly Automated Driving

17:00 Nobuhiro Hosokawa, Research Laboratory, Japan, How to assure the software quality for Artificial Intelligence?

17:30 Panel discussion with the lecturers

20:00 Dinner

Friday July 07: Deep Learning & NN

Session 17: Keynote

08:30 Ren Wu, NuvoMind, USA, *I*²*OT-Embedded Vision and Embedded Intelligence*

09:30 Break

Session 18: In-Depth Presentations

10:30 Yuan Xie, UCSB, USA, Technology-driven and Application-driven Architecture Innovation: Past, Present and Future

11:00 Shintaro Yamamichi, Tokyo Research Laboratory, Japan, *Neuromorphic hardware* research for Cognitive Computing

11:30 Song Yao, DeePhi Tech, China, BandwidthCentric Deep Learning Processing through Software-Hardware Co-Design

Session 19 : Mini-Keynote Presentations

12:00 Nicolas Ventroux, CEA-List, France, **N2D2**: *An Open-Source Design Environment For DNN*

12:12 Frédéric Petrot, TIMA, France, Scalable
High-Performance Architecture for Convolutional
Ternary Neural Networks

12:24 Panel discussion with the lecturers

13:00 Lunch