KONICA MINOLTA

Designing Structure of Image Processing in MFP

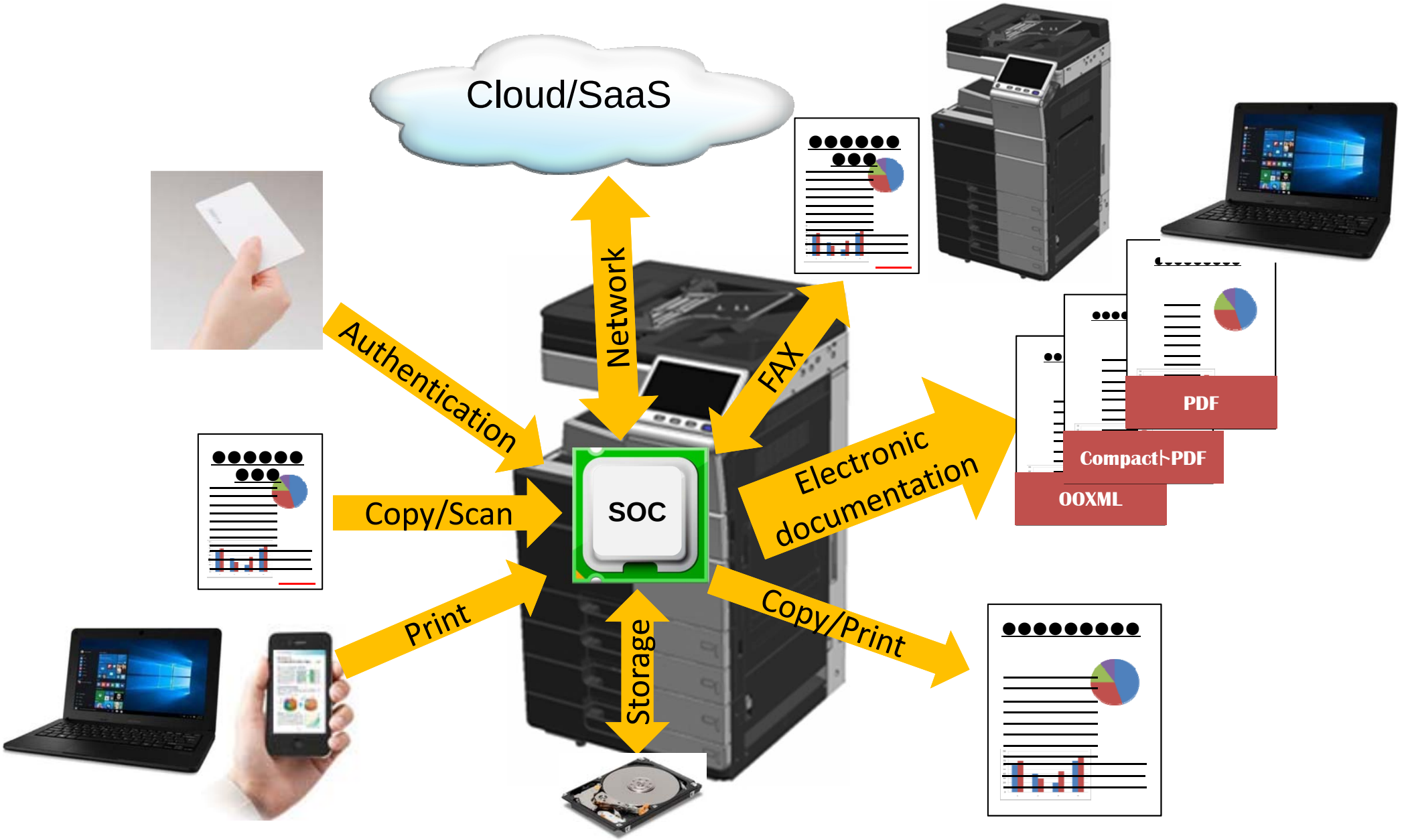
「複合機におけるイメージ・プロセシングの設計構造」

MPSoC'17

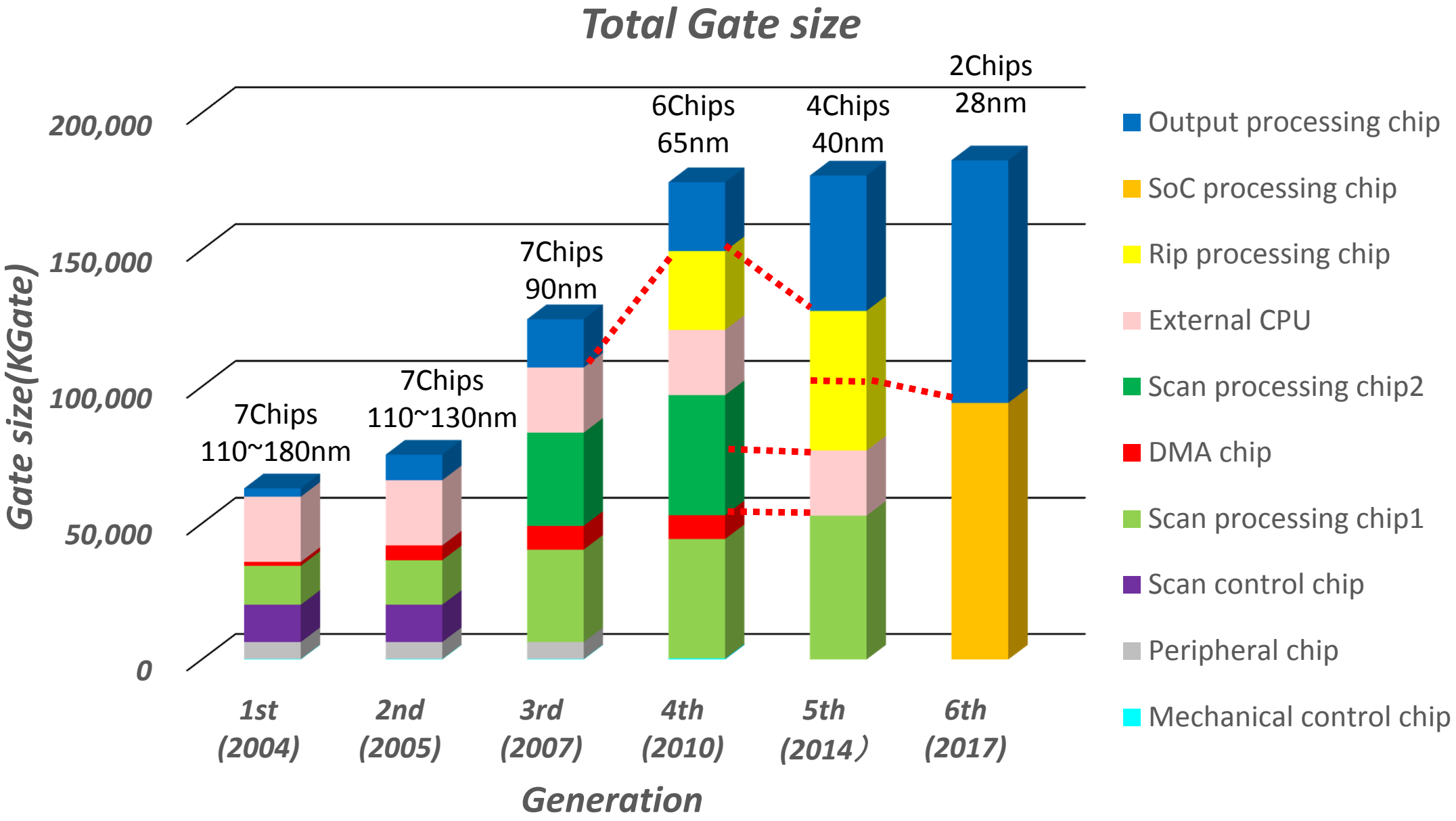
July 6th, 2017

Table of Contents

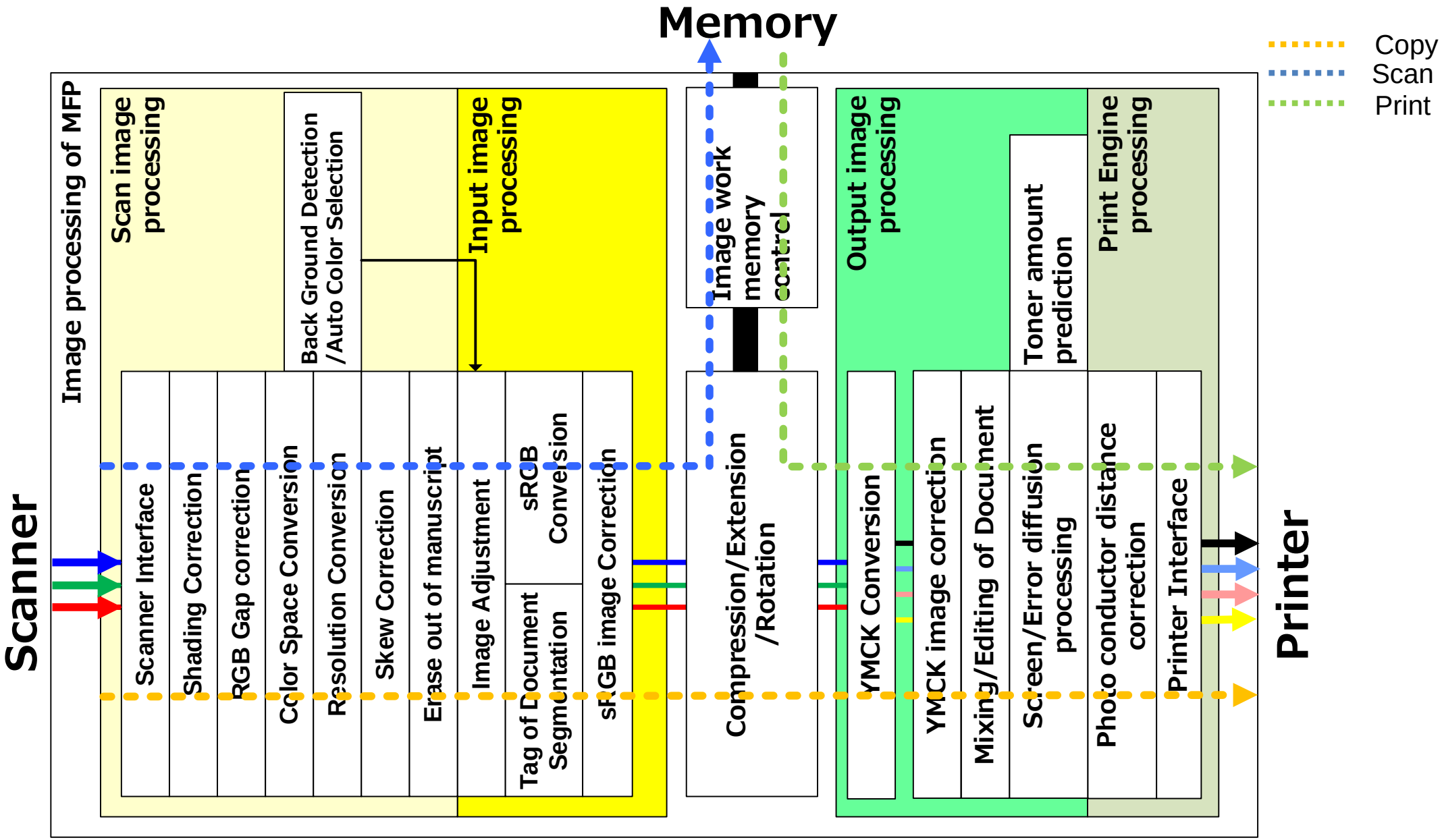
1. Image Processing Functionality of MFP



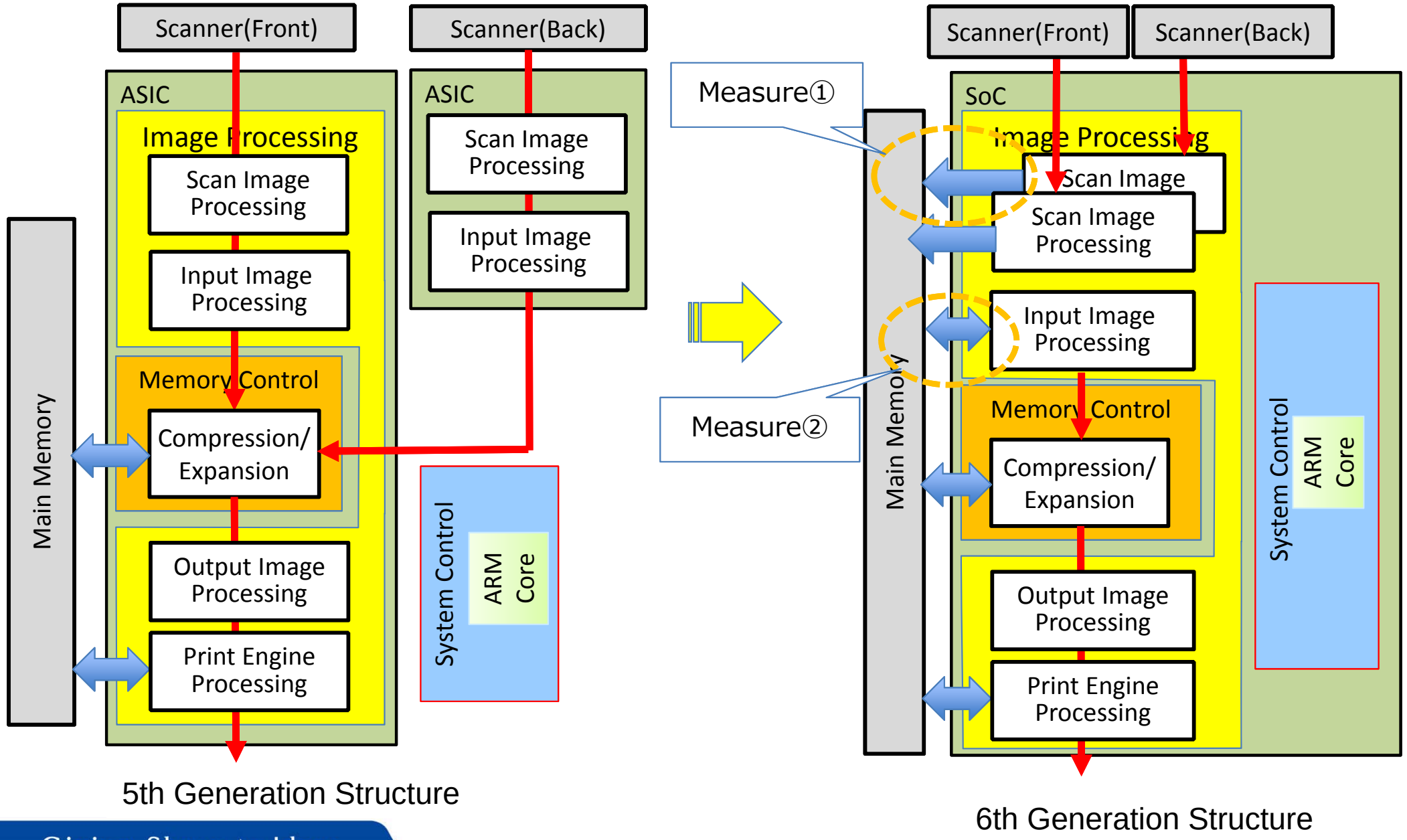
2. Trends of ASIC Size



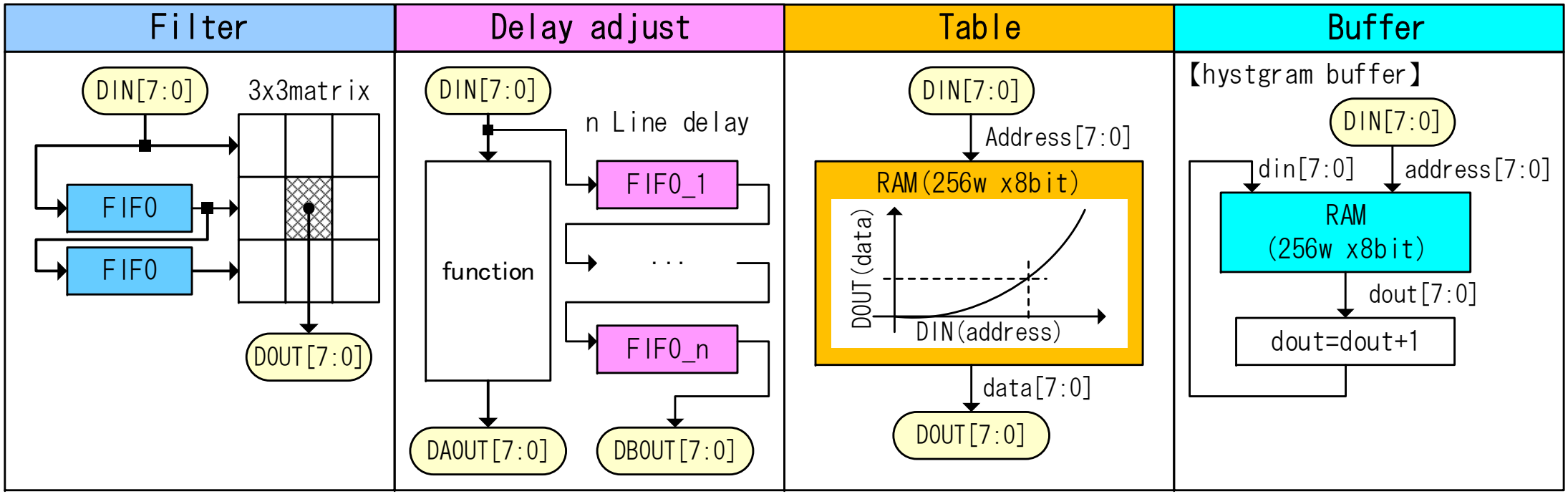
3. Block Diagram of Image Processing Flow



4. Structure of Image Processing

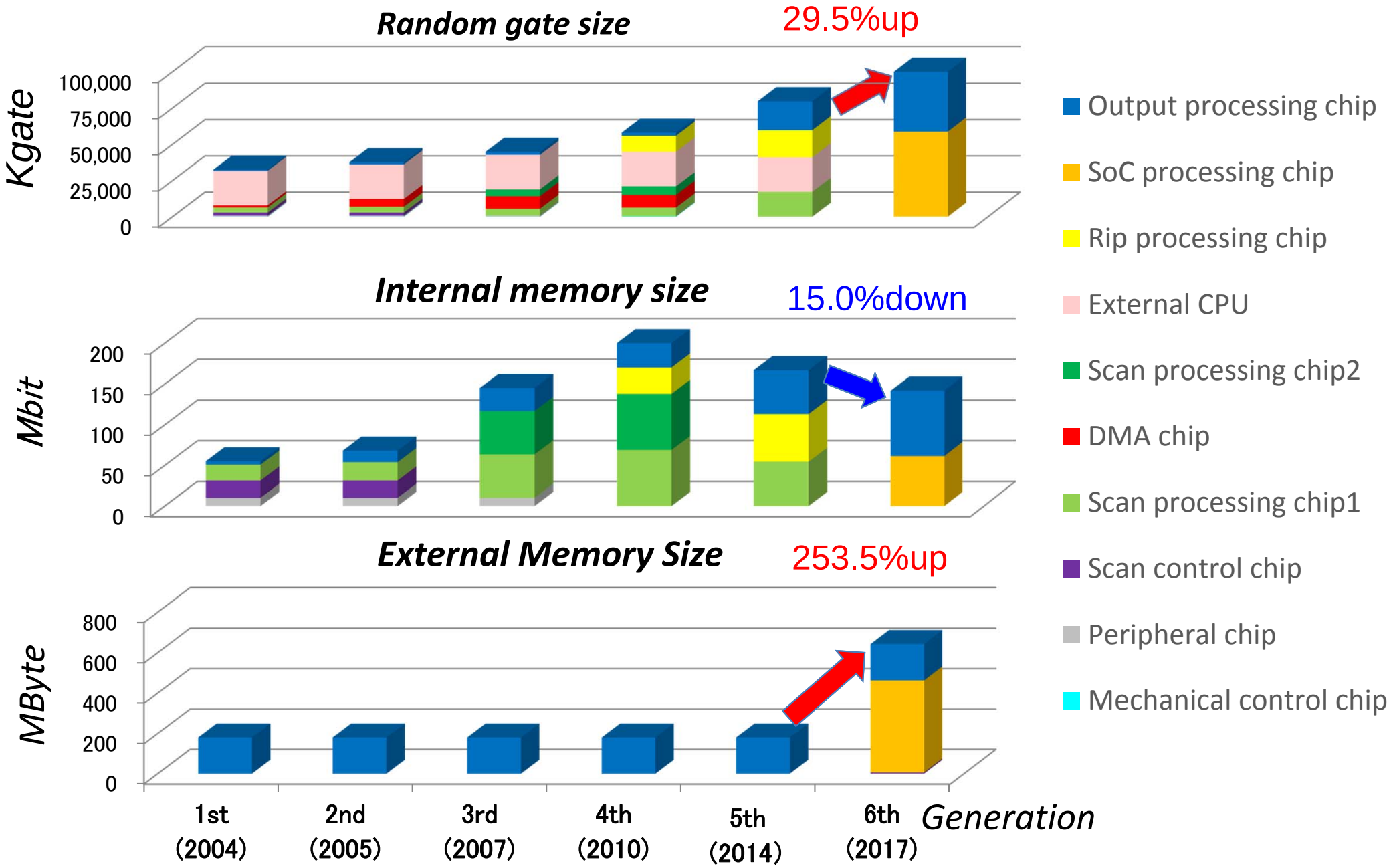


5. Using Method of Memory in the Image Processing

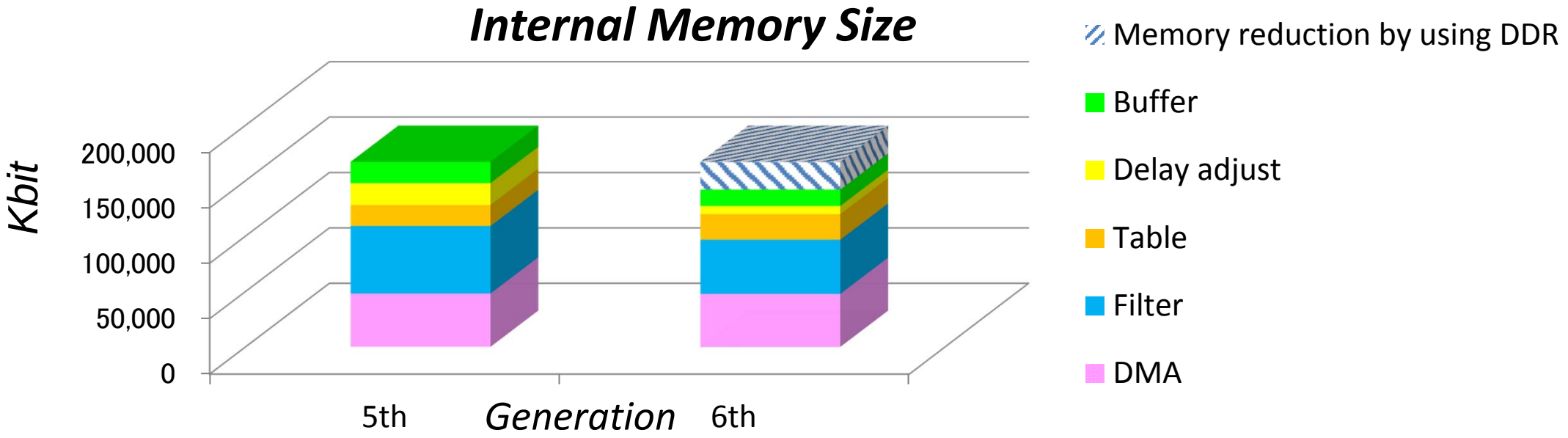


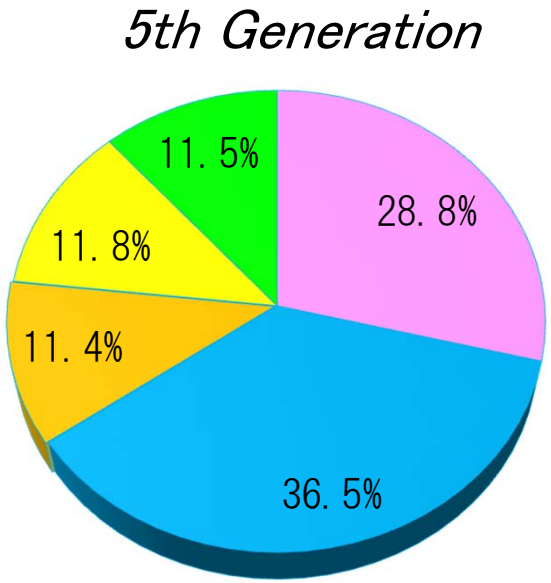
- *Filter-type : Space filter processing based on the FFT.*
- *Delay adjust-type : Delay adjustment among image processing modules.*
- *Table-type : Characteristic conversion of image data.*
- *Buffer-type : Memory cell for image processing operation.*

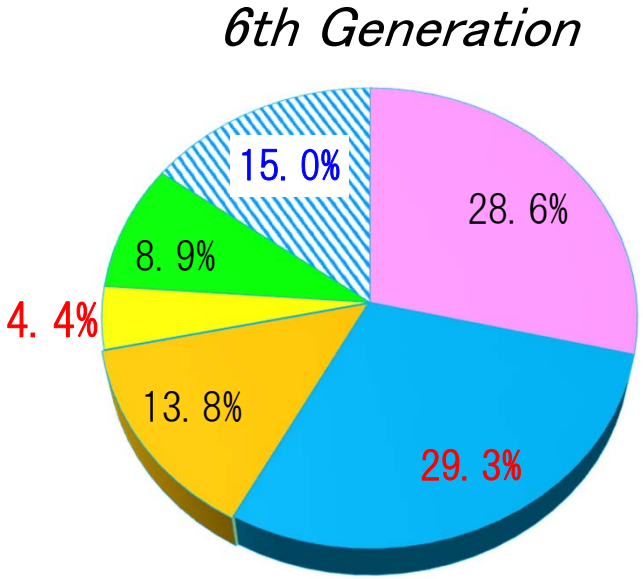
6. Trends of Random Gate and Memory Size



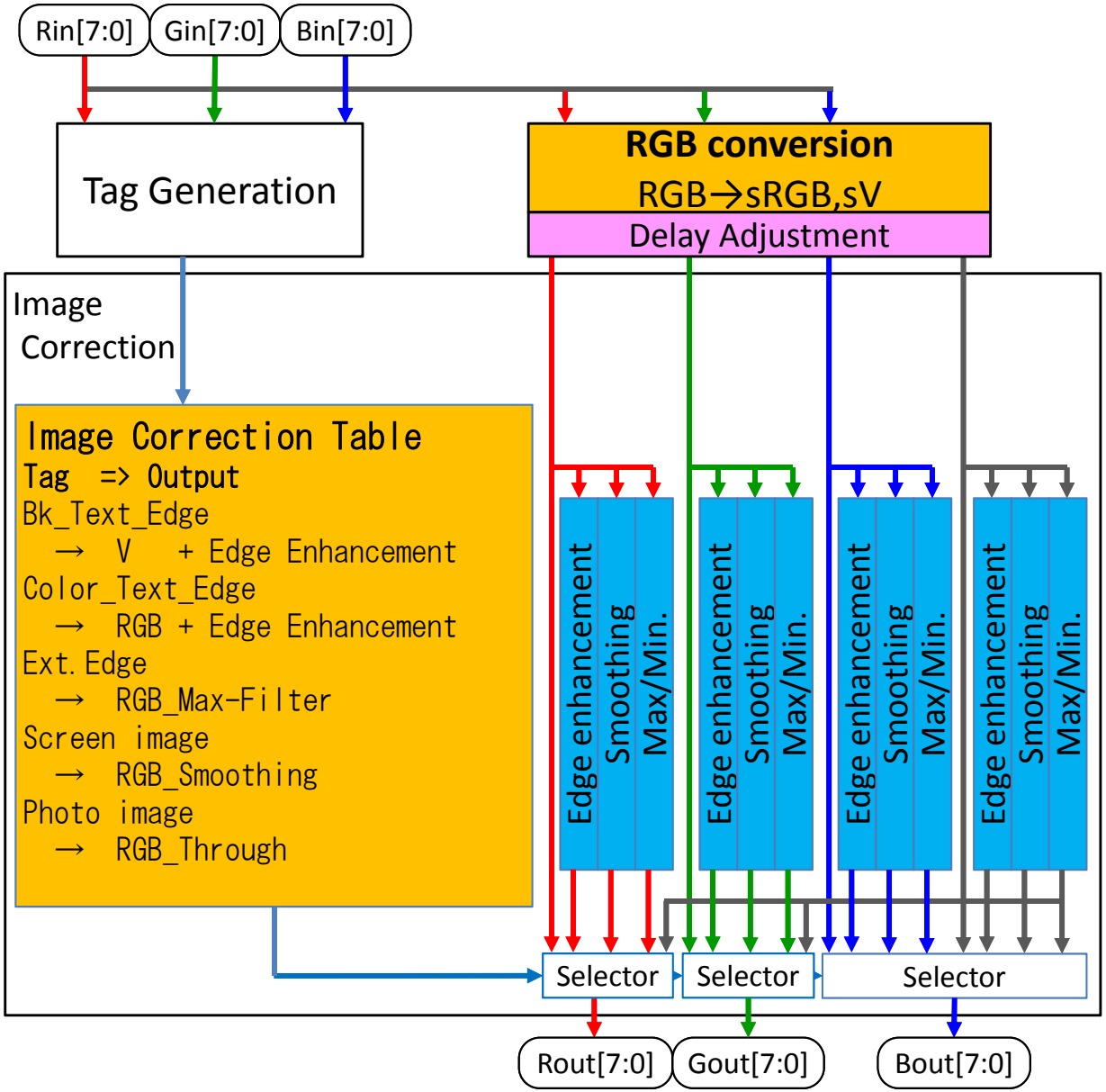
7. Percentage of Memory-type in the Image Processing

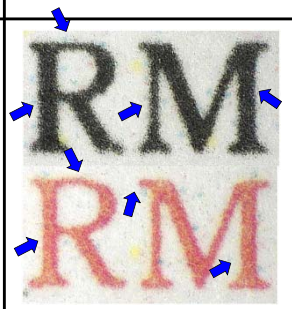
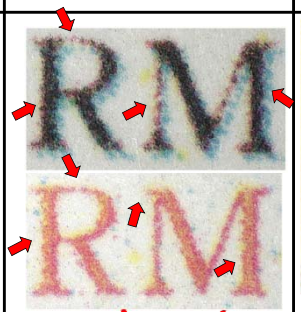






8. Tag Generation & Image Correction of Documents



		Text	Screen Image	Photo Image
Original (RGB)		RM RM		
Image Correction	ON	 Sharp Line	 Smooth	
	OFF	 · Broken Line · Color Blur	 · Jaggies · Moire	

9.Document tag generation

Rin[7:0] Gin[7:0] Bin[7:0]

Document tag generation

Edge Detection

Edge Boundary Detection

Screen Image Detection

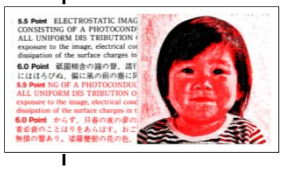
Line Pair Detection

Color Area Judgment

Delay Adjust

Delay Adjust

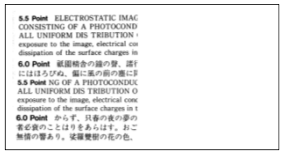
Delay Adjust



RGB conversion RGB→sRGB,sV

Delay Adjust

Text Judgment



Document Tag Generation

Tagout

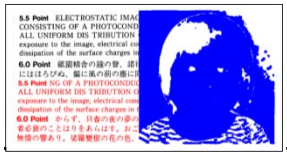
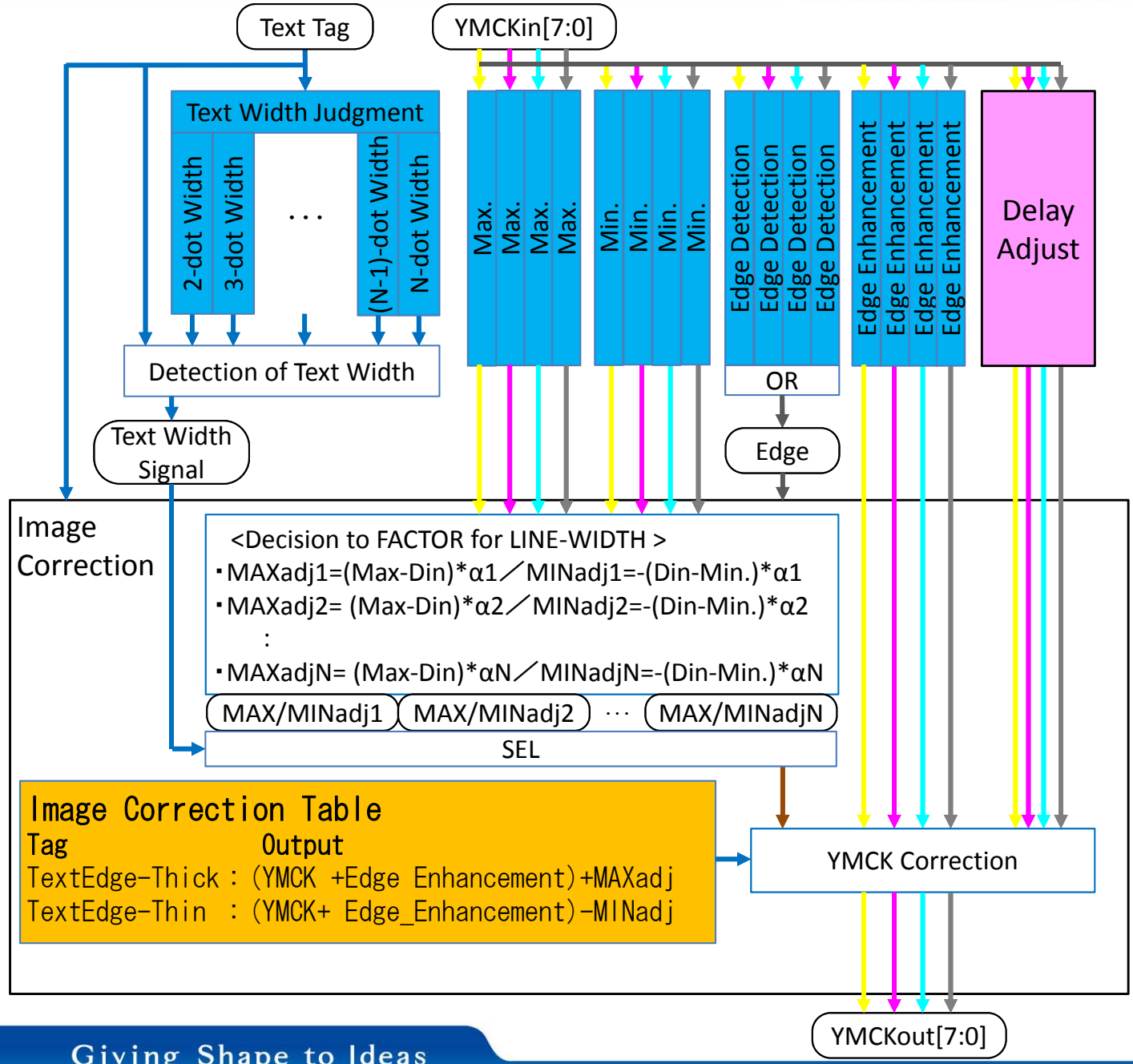


Image Correction

Rout[7:0] Gout[7:0] Bout[7:0]

10. Detection of Text-line Width

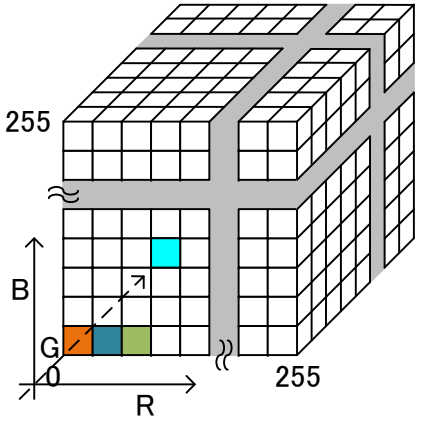


Correction Level	Black Text	Color Text
Normal	RGB	RGB
	RGB	RGB
Thin	RGB	RGB

11.Color-Space Conversion

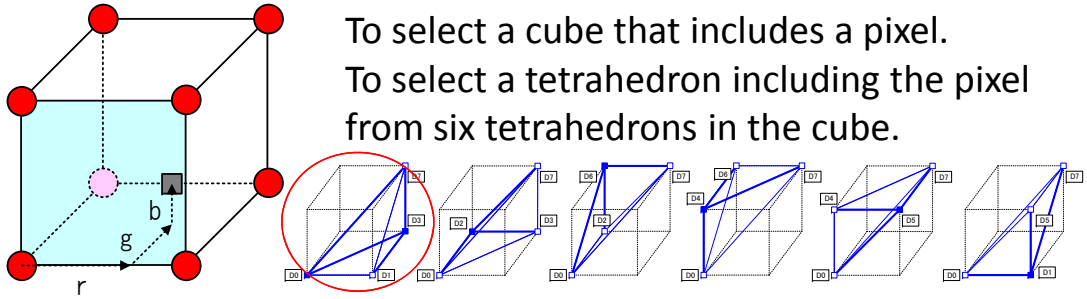
KONICA MINOLTA

Step1. Color space mapping



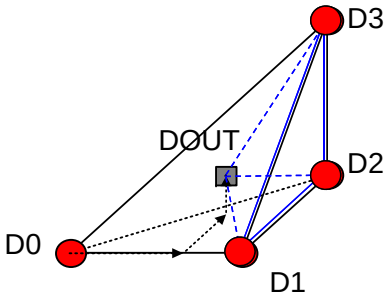
To divide RGB space of 256 gradations into the RGB space (cubes) of 16 gradations.
To save data of the eight vertexes on the cubes into memory.

Step2. Search cube and tetrahedron mapping



To select a cube that includes a pixel.
To select a tetrahedron including the pixel from six tetrahedrons in the cube.

Step3. Tetrahedral interpolation

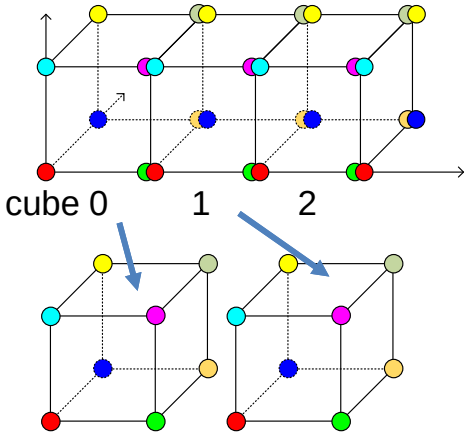


To calculate each volume of four spaces among four points (DOUT-D1-D2-D3,DOUT-D0-D2-D3, DOUT-D0-D1-D3 and DOUT-D0-D1-D2)
T0=Volume of space among DOUT,D1,D2,D3.
T1=Volume of space among DOUT,D0,D2,D3.
T2=Volume of space among DOUT,D0,D1,D3.
T3=Volume of space among DOUT,D0,D1,D2.

DOUT = (T0*D0 +T1*D1 +T2*D2 +T3*D3)/(T0+T1+T2+T3)

[Technique for data compression]

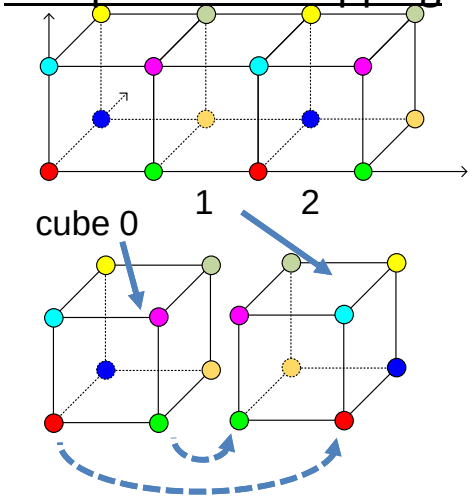
Normal mapping



LUT0 LUT4
LUT1 LUT5
LUT2 LUT6
LUT3 LUT7

39,304 byte/LUT0~7
(=17x17x17x8)

Compression mapping



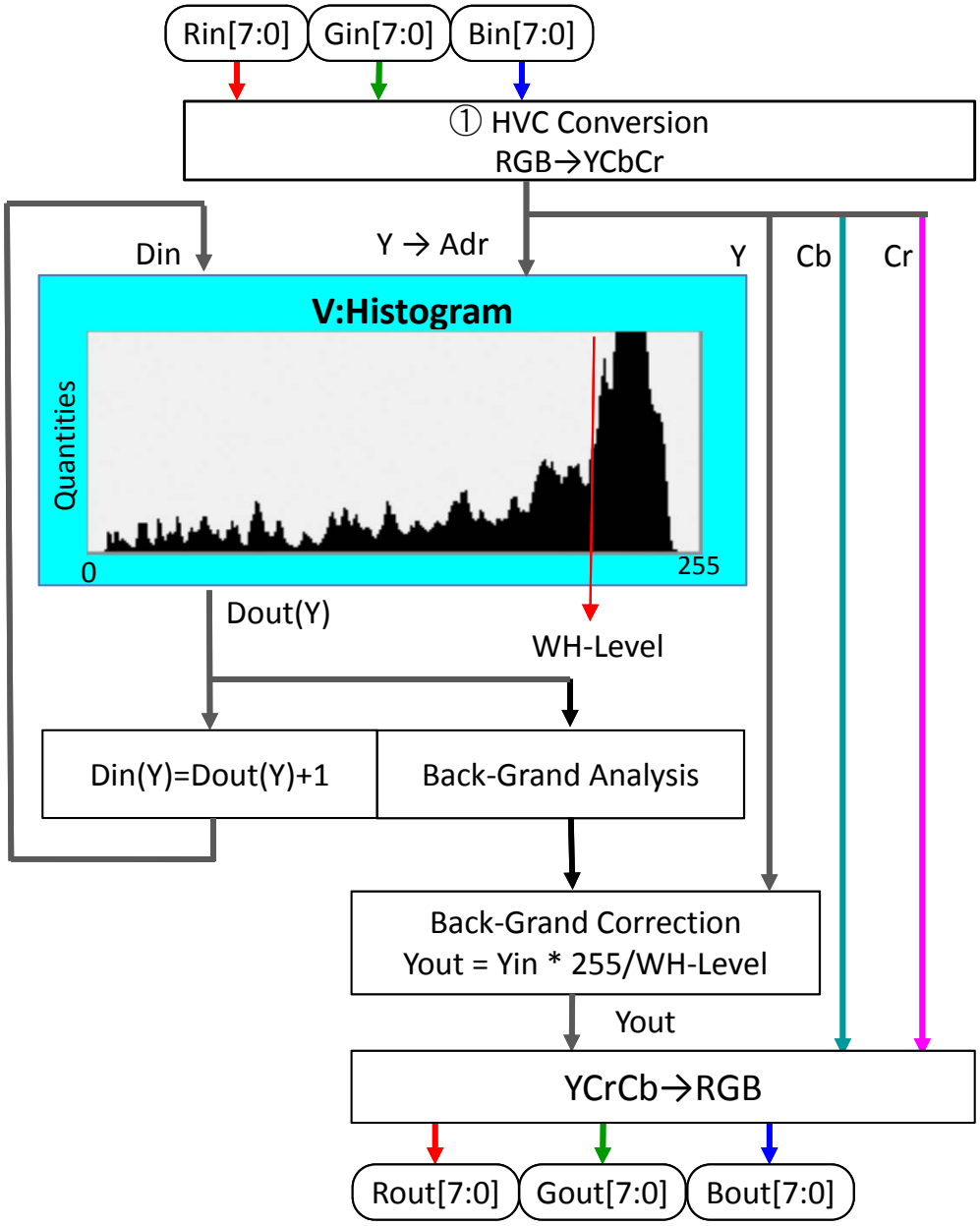
LUT0 LUT4
LUT1 LUT5
LUT2 LUT6
LUT3 LUT7

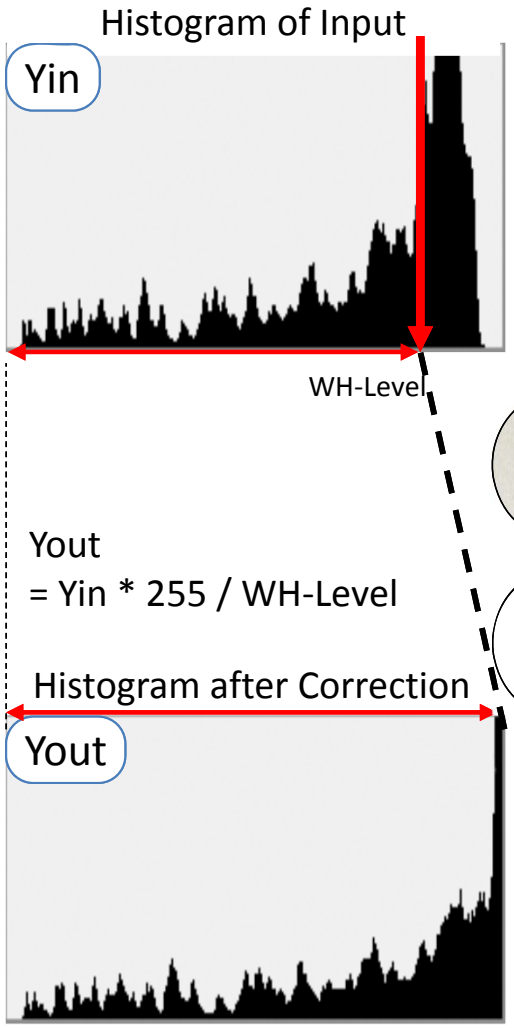
729 byte/LUT0 (=9x9x9)
648 byte/LUT1,2,4(=9x9x8)
576 byte/LUT3,5,6(=9x8x8)
512 byte/LUT7 (=8x8x8)

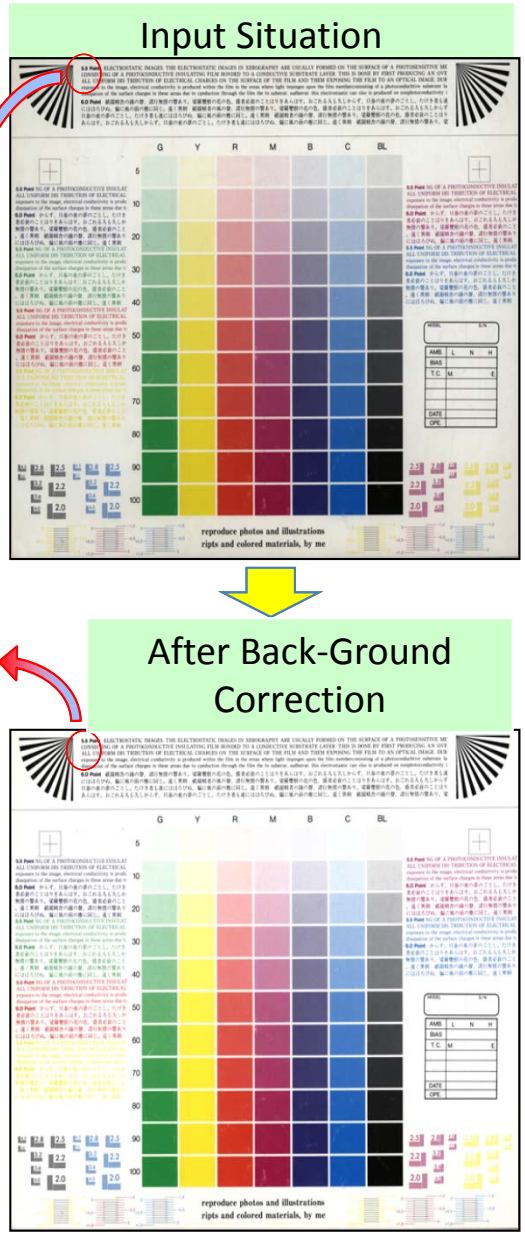
Total:4,913byte/LUT0~7

Compression ratio : 12.5%

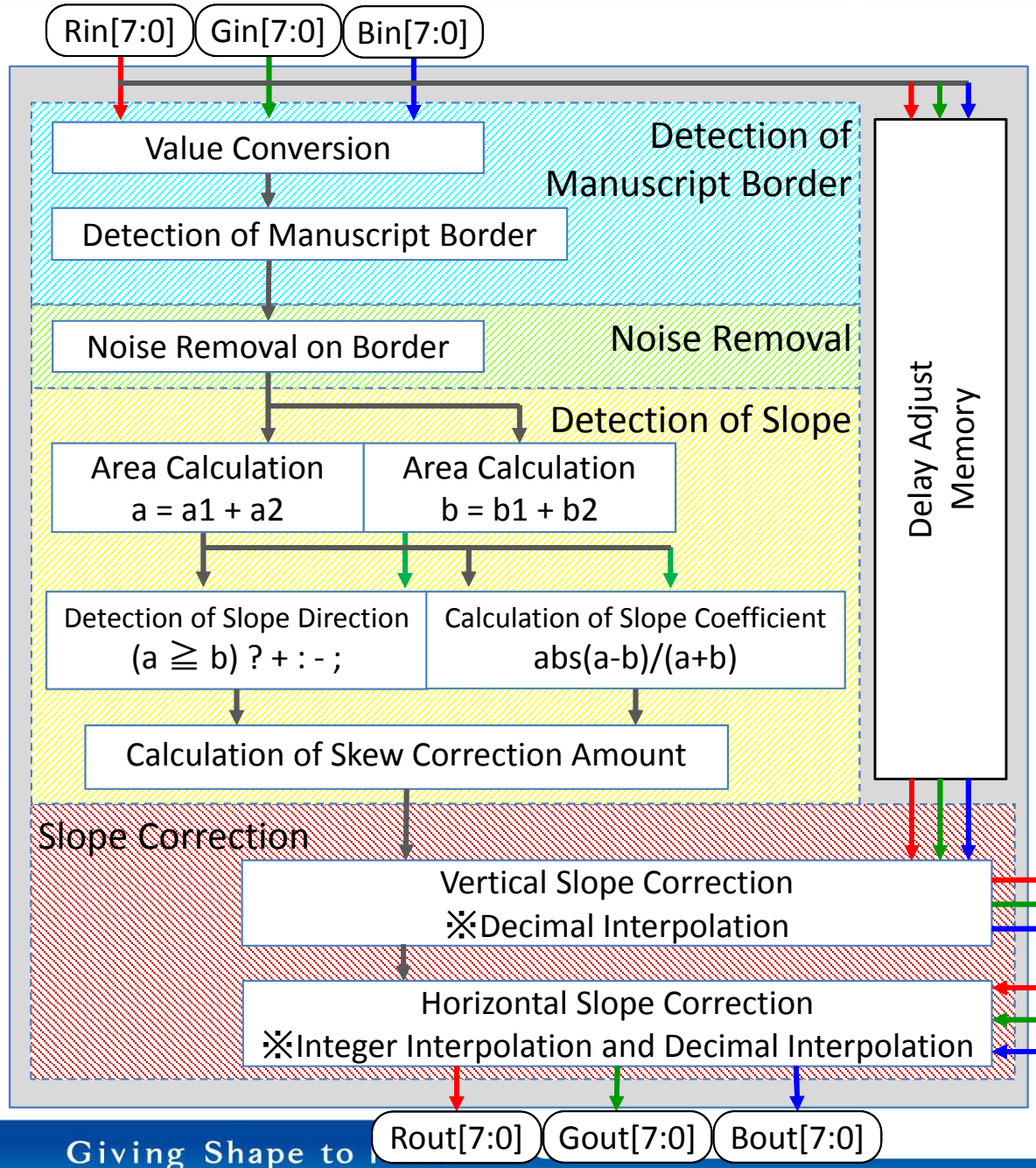
12. Automatic Correction of Background-Level

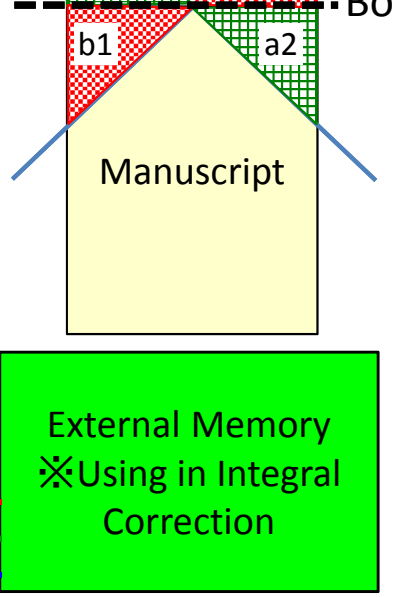






13. Image Skew Correction



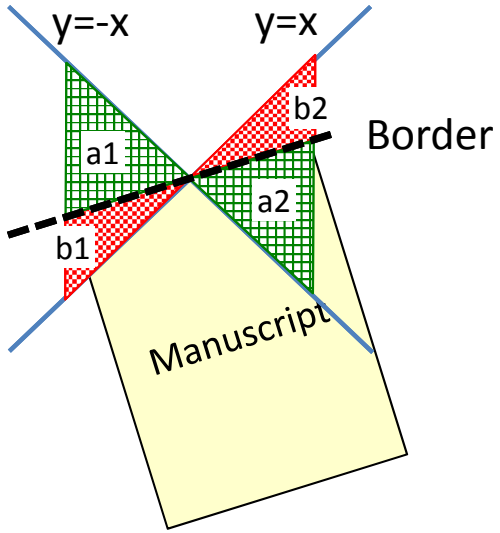


Non skew
- a = b
- abs(a-b)/(a+b) = 0

※a=a1+a2, b=b1+b2

Skew left
- a < b
- abs(a-b)/(a+ b) ≠ 0

※a=a1+a2, b=b1+b2



14.Effect of Image Skew Correction

Scan input(skew : θ)

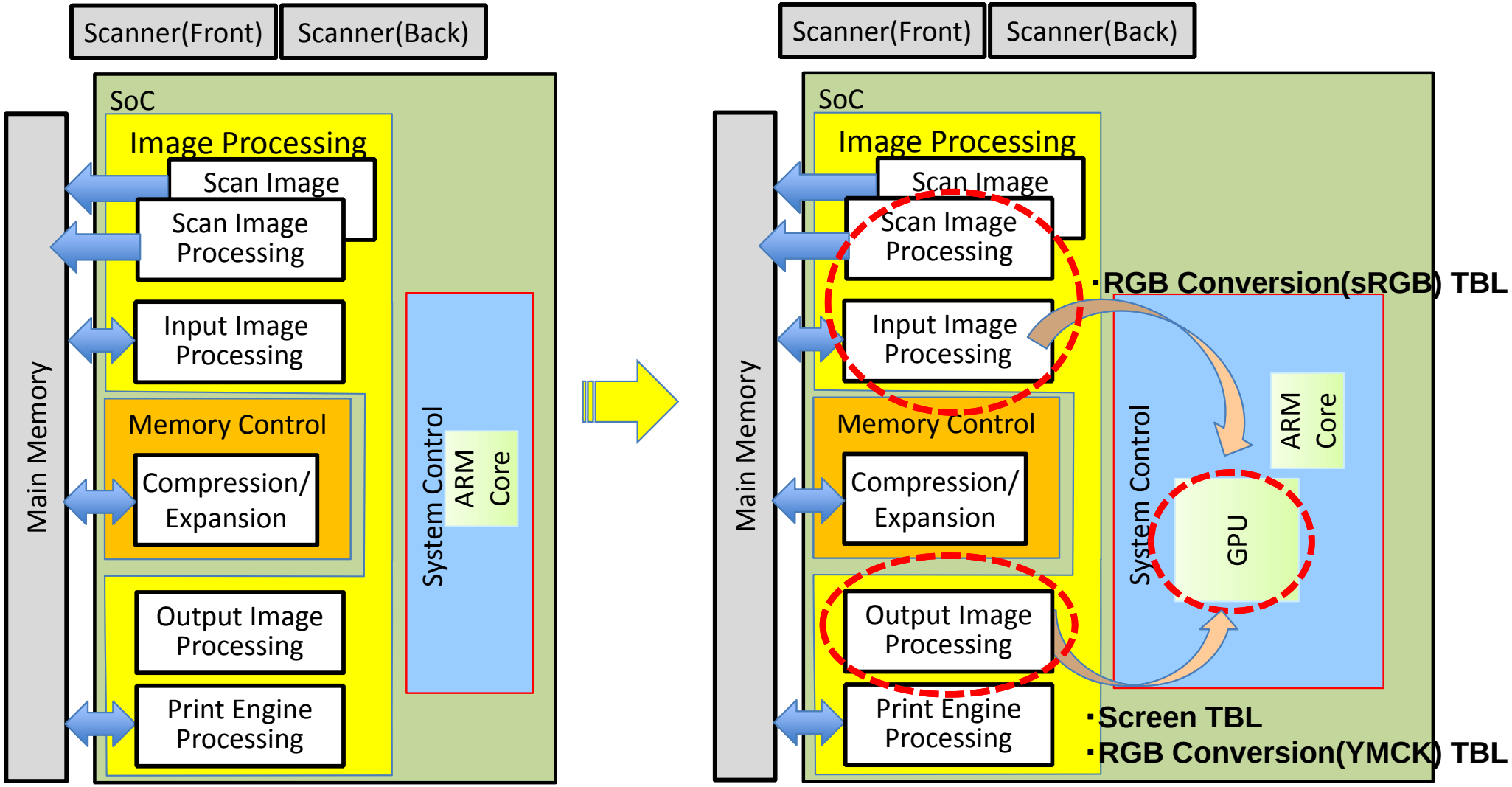
Low resolution correction

NG: discontinuity of image

High resolution correction

- Resolution step: 1/4096
- Skew adjustment: Bi-cubic

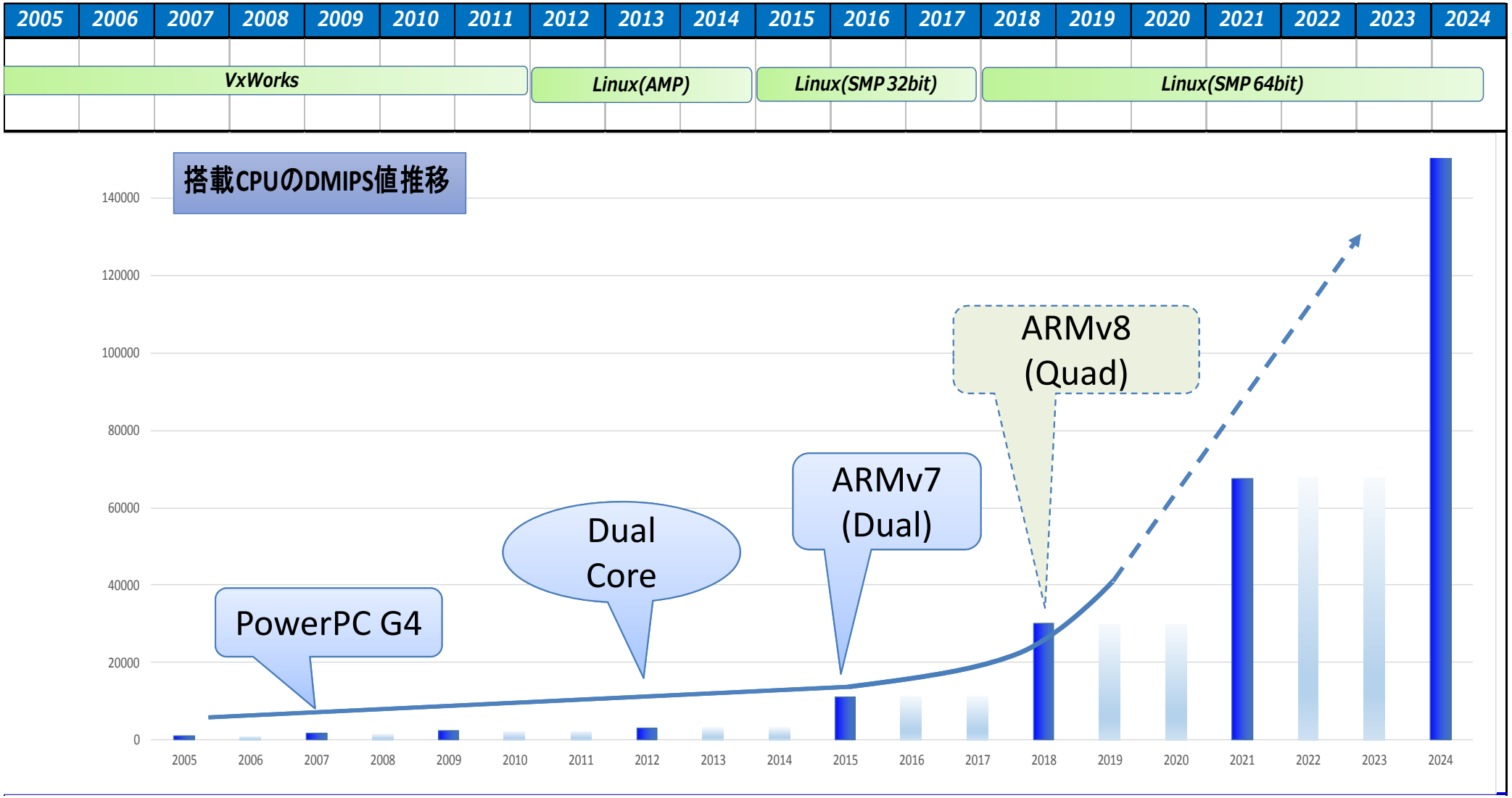
15.Next Generation Structure



6th Generation Structure

Next Generation Structure

16. Trends in the CPU Performance of MFP



17. Utilize GPU in the future

To cover Image-processing Function in MFP

1) Converting to the File Formats of Scan Document
(Compact-PDF／Searchable-PDF)
- ➡ *Layer separation and Integration*
- ➡ *Separation of Text-Area and Graphic-Area*

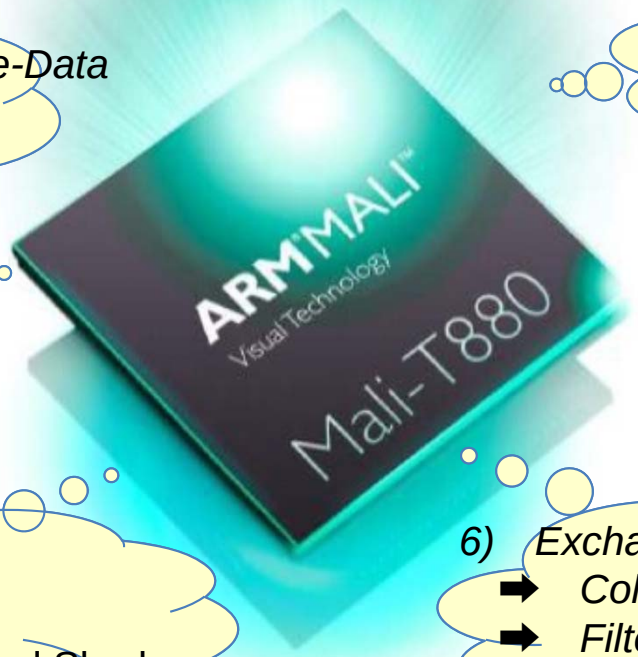
2) Compression & Extension of the image-Data
- ➡ *Display on the LCD-Panel*
- ➡ *Jpeg-Conversion*

3) Rasterization of RIP-data
- ➡ *Rendering, Texture filtering,* Pixel Shader

4) Instruction with Animation of MFP-Operation

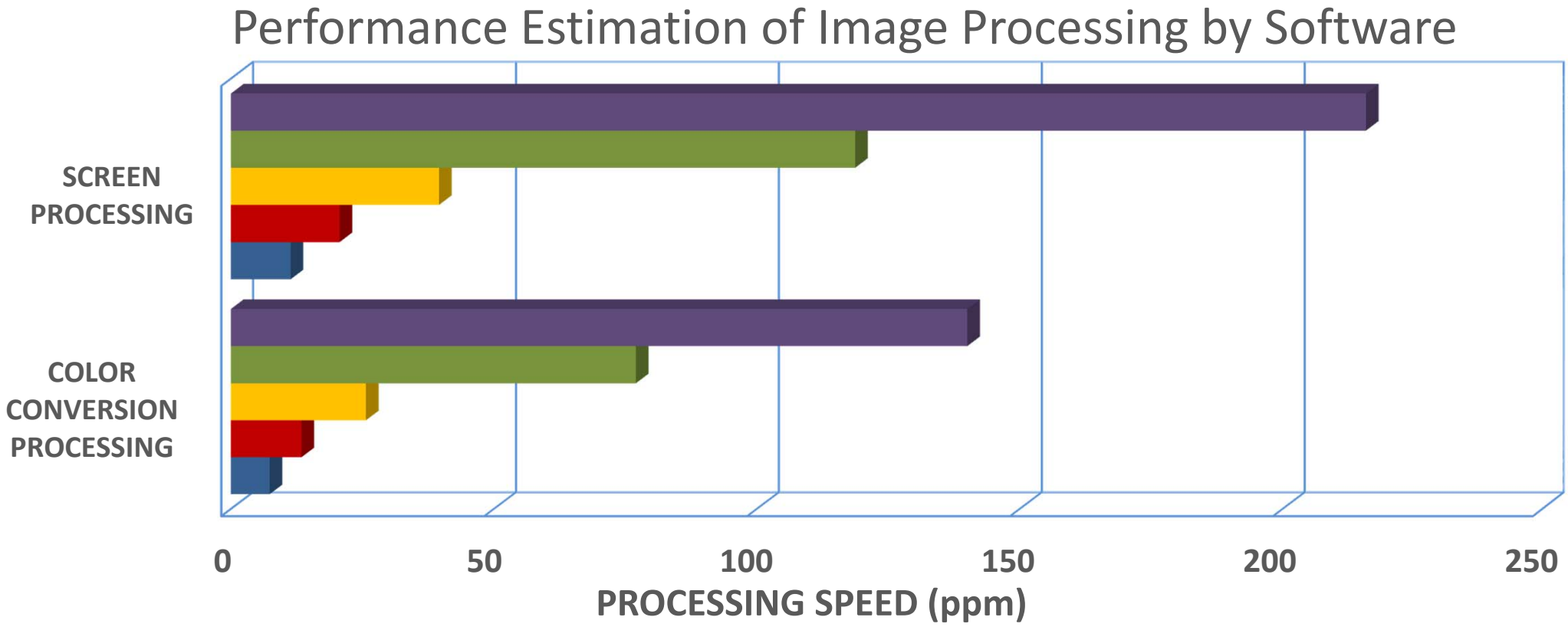
5) Mixing of the Documents
- ➡ *Water-Mark*
- ➡ *Overlapping of The Documents*

6) Exchange From HW-image-Processing Module
- ➡ *Color-Space Conversion*
- ➡ *Filtering*
- ➡ *Reproduction Processing for Printing*



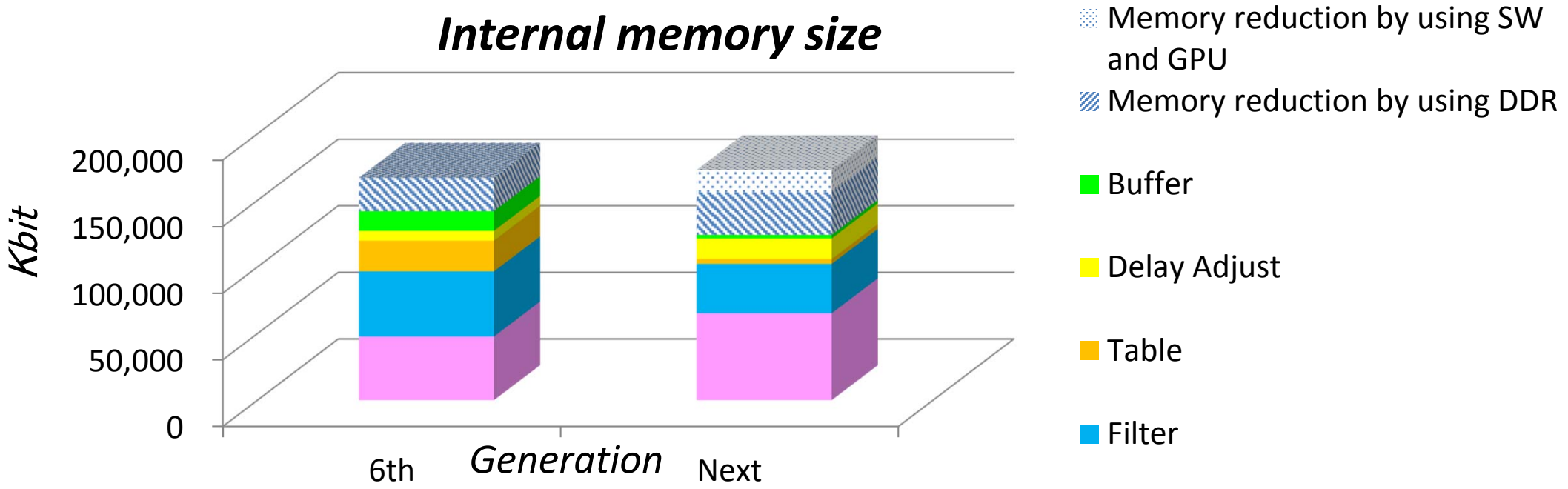
18. Performance by Changing Processing from HW to SW

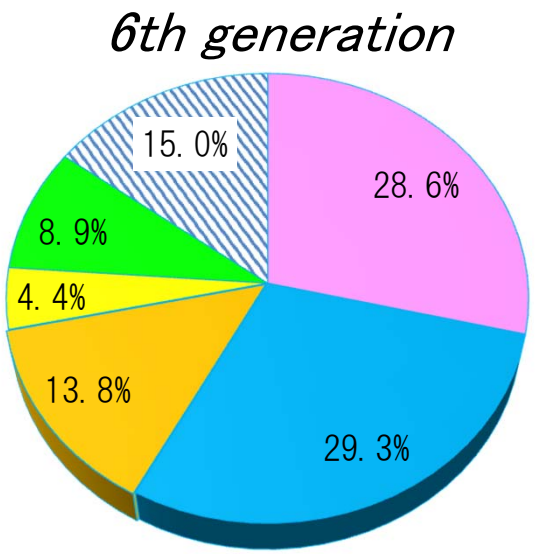
KONICA MINOLTA

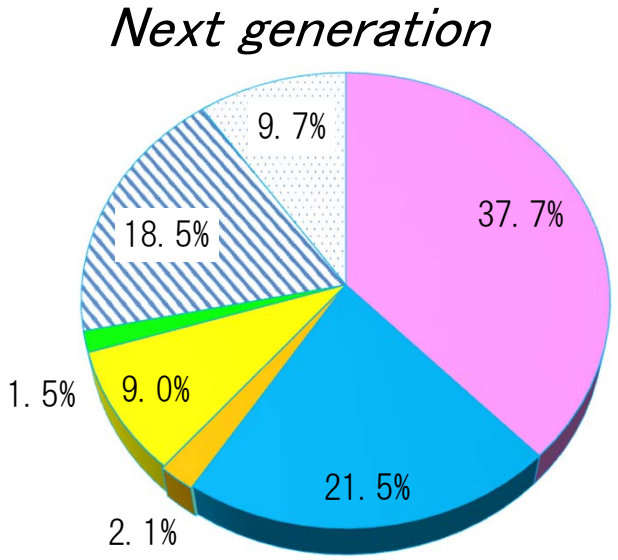


- Case1: Sequential processing on CA72 Single Core@1.6GHz Single Core
- Case2: Parallel processing on CA72 Dual Core @1.6GHz
- Case3: Parallel processing on CA72+SIMD Dual Core @1.6GHz
- Case4: Parallel processing on Next Gen CPU+SIMD Dual Core @2.2GHz
- Case5: Parallel processing on Next Gen CPU+SIMD Dual Core @2.2GHz and GPU(SC=8~16)

19. Memory reduction in next generation







Merci pour votre attention

Thank you very much!

Abstract:

Hardware architecture that is employed on MFP controller is realized by integrating 3 function blocks; 1. Controlling function using ARM core that is applied to devices such as Smartphone, 2. Memory controlling function that inputs, deliveries, prints and storages image, 3. Imaging processing function that corrects, edits and converts imaging data, and then making SoC.

When thinking of employment technology of system controlling function, how fast you can acquire and use leading-edge technology is an important R&D requirement. However, since it has generic architecture following technology trend of semiconductor as its base, there is no technology difference between companies, and so the commoditization is in progress. Also, looking at memory controlling function, architecture itself has the same function with generic data bus technology represented by PCI-Express even image data compression and decompression technology differ from company to company.

On the other hand, looking at imaging processing function, each company develops unique algorithm from the early stage of MFP digitizing to make a hardware as a design asset to improve its performance and function. This hardware asset is a combined structure of controlling functions of large-sized and divided local memory group and pipe-line following image processing flow, and the structure can be looked very unique when looking from other industries.

In this report, we are focusing on the imaging processing in MFP and explaining the background of our R&D and future direction from a viewpoint of ASIC design.

Main Contents:

- Gate size of ASIC/SoC development, change of memory capacity
- Basic block and image flow of image processing
- Method of using memory in image processing function
- Future direction of image processing function

Abstract:

タイトル:「複合機におけるイメージ・プロセシングの設計構造」

複合機のコントローラに採用しているハードウエア・アーキテクチャーは、「スマートフォン等に搭載されているARMコアを使ったシステム制御部」に加え、「画像データを入力，配信，プリント，ストレージするためのメモリ制御部」および「画像データを補正・編集・変換するためのイメージング・プロセッシング部」の3つの機能ブロックを統合し、SoC化することで実現している。

システム制御部の採用技術は、最先端テクノロジーをいかに早く使いこなすかが重要な開発要件だが、半導体の技術動向に追随した汎用アーキテクチャーがベースであるため、各社の違いがなくコモディティ化している。 また、メモリ制御部も各社が採用している画像データ圧縮・伸長技術は異なるものの、PCI-Expressに代表される汎用的なデータ・バス技術を活用することで、アーキテクチャーそのものは同じ形態になっている。

しかし、イメージング・プロセッシング部は、複合機のデジタル化初期段階から、各社固有のアルゴリズムを開発し、ハードウエア化による設計資産をベースに性能・機能を進化させている。 このハードウエア資産は、大規模で分割されたローカルメモリ群の制御と画像処理フローに沿ったパイプライン制御を組み合わせた構造となっており、他の業界から見ると非常にユニークな構造になっている。

本報告では、複合機のイメージング・プロセッシングにフォーカスをあて、ASICデザインの視点から、これまでの開発経緯と今後の方向性を述べる。